Medium Voltage SiC Based Power Electronics Design and Control for Grid Applications

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Centre for Power Electronics Annual Conference
University of Nottingham
July 4-5, 2023

Tennessee – The Energy Valley

- Manhattan project
- Oak Ridge National Lab
- TVA, EPRI
- UTK

CURENT

THE UNIVERSITY OF TENNESSEE KNOXVILLE

CURENT UTK at a Glance

- CURENT was established in 2011 as a 10 year $40M US NSF/DOE Engineering Research Center, the first US DOE-NSF ERC and only one with a power system focus
- CURENT involves four US institutions with about 25 faculty members and 100 graduate students
- UTK is the lead institution with 10 core faculty members in power systems and power electronics, four affiliated faculty, about 80 graduate students with mostly PhD students, a number of post docs, and undergraduate students
- 35 industry and government partners
- Close collaboration with Oak Ridge National Lab

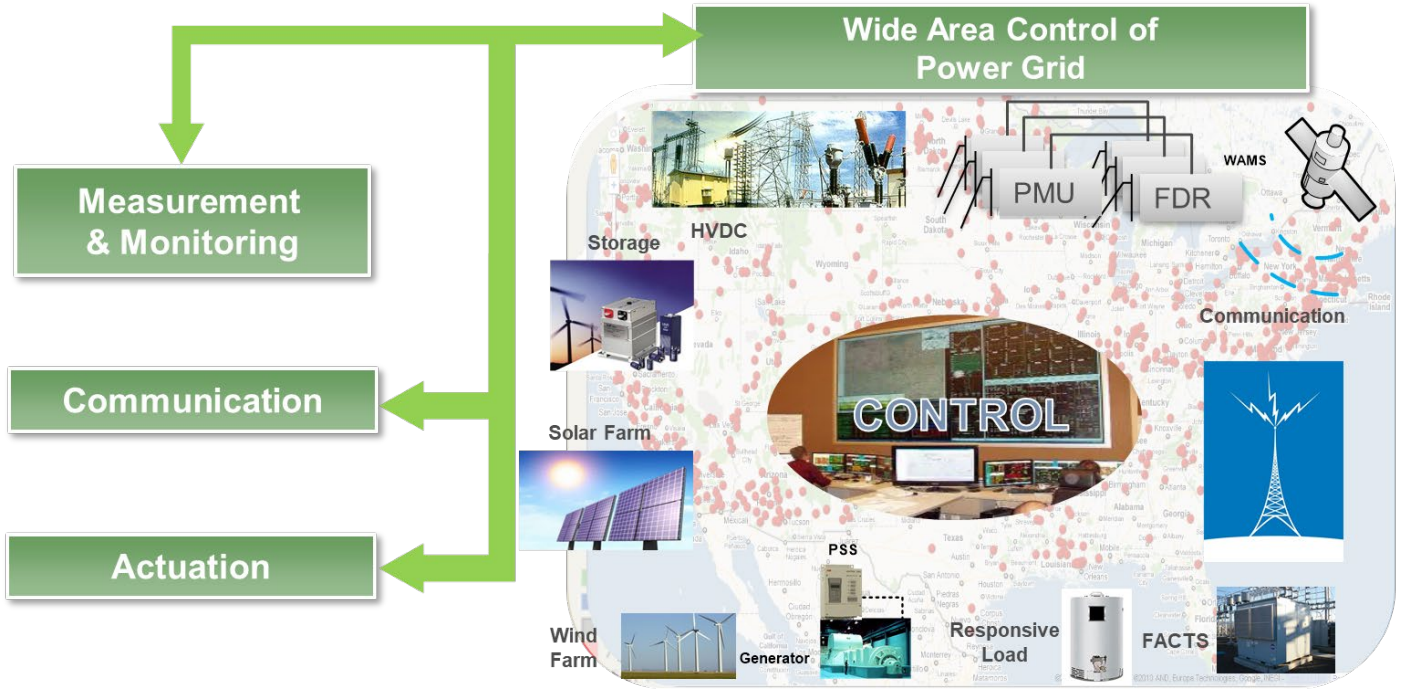
CURENT Research Scope

Original Vision

- Monitoring, modeling, control and actuation of a nation-wide transmission grid for high efficiency, high reliability, low cost, better accommodation of renewable sources, full utilization of storage, and responsive load.

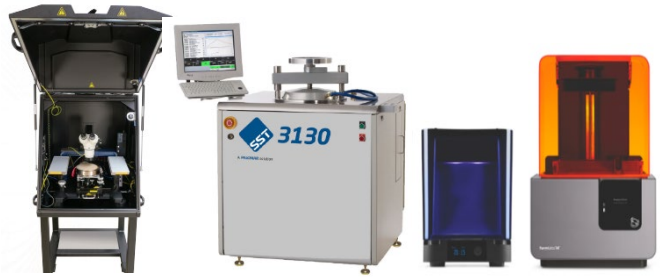
Expanded Scope

- Transmission & distribution grids
- Microgrids
- Energy storage
- Electrification of transportation and other systems
- AI applications for electrical systems
- Power electronics components, converters, & systems



UTK CURENT Facilities

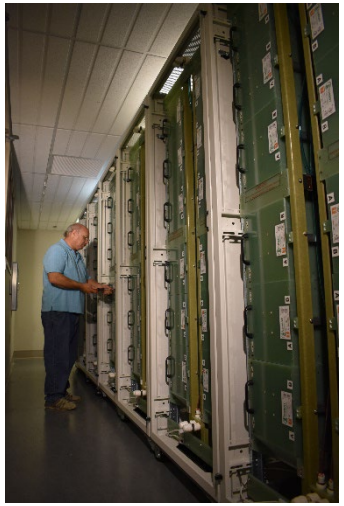
Low and Medium Power Lab



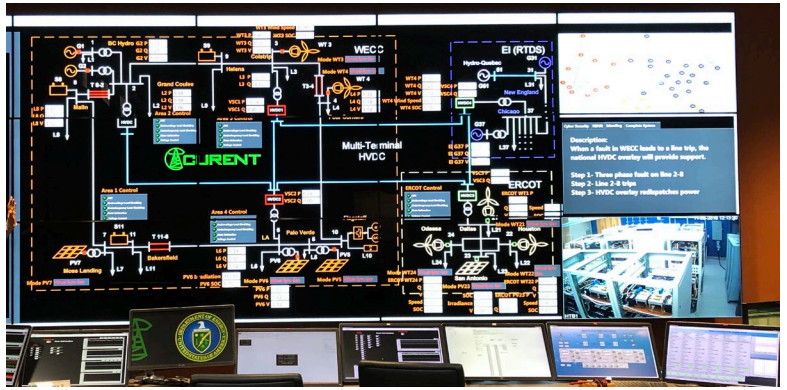
Packaging Lab Equipment

Conference Room

High Power Lab



MV MW Tester



Visualization and Control Lab

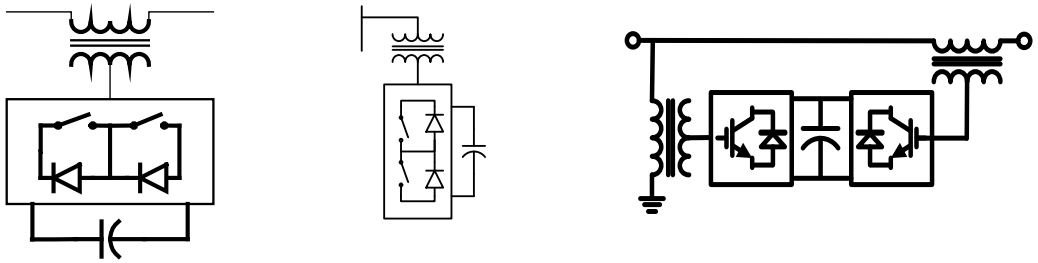
Grid Emulation Lab - HTB

MV SiC Power Electronics Presentation Outline

- ❑ Overview
- ❑ Benefits of MV SiC Power Electronics for Grid Applications
- ❑ MV SiC Power Electronics Converter Design Considering Grid Requirements
- ❑ Some Example Design and Control Issues
- ❑ Summary

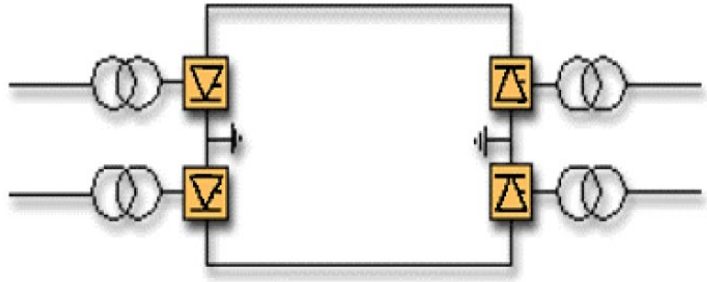
Grid Applications Call for MV/HV Power Electronics

- **AC Transmission & Distribution**

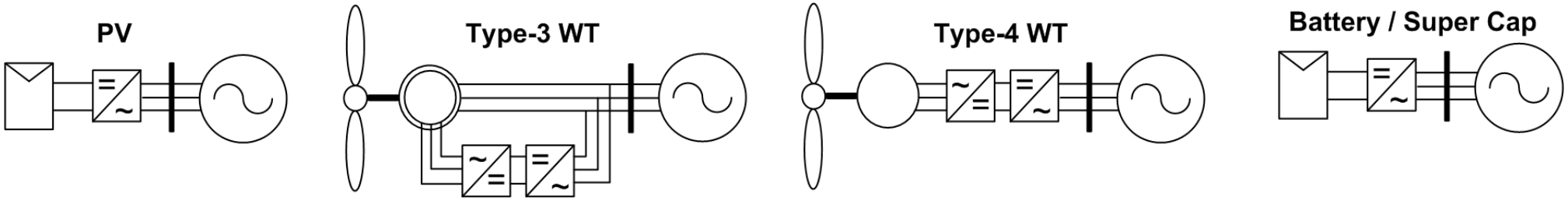


Series/shunt compensation or power conditioning

- **HVDC/MVDC**



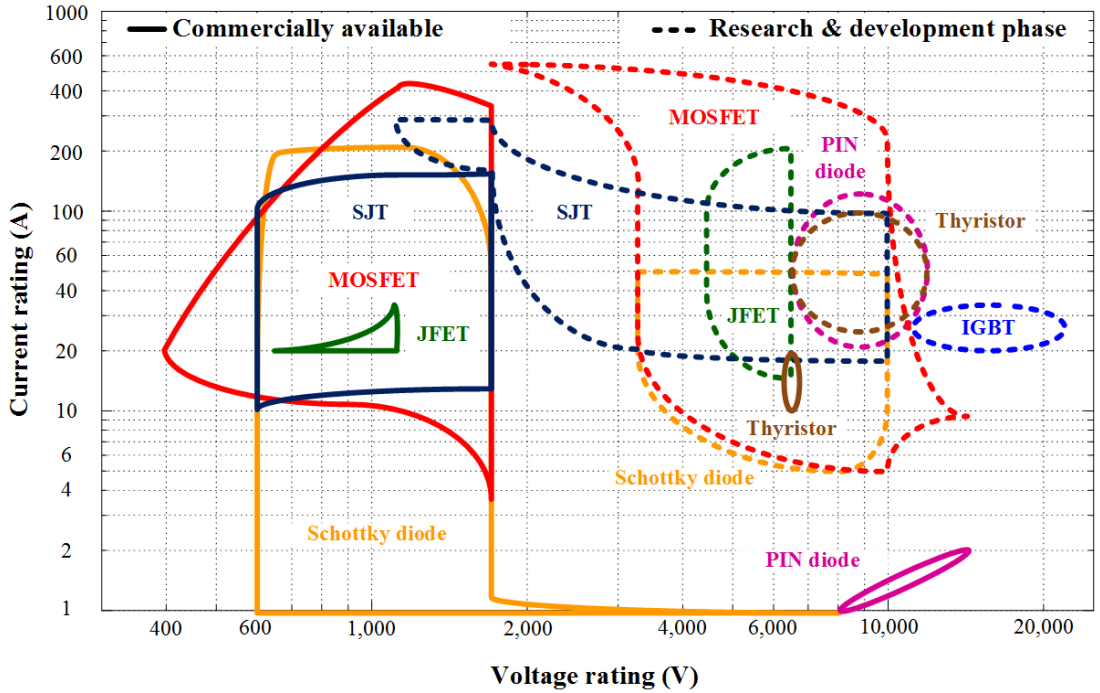
- **Renewable energy source and energy storage interface**



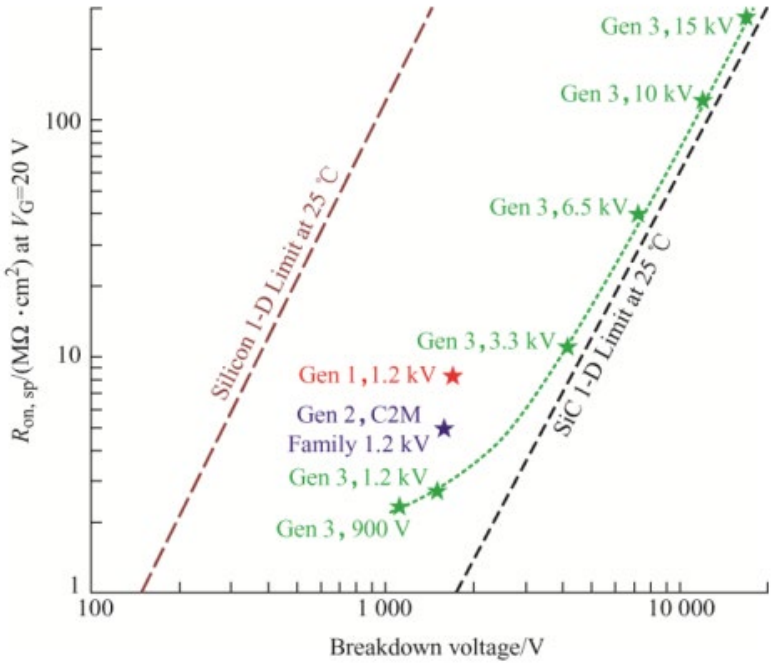
- **Large power electronic loads (data centers, EV charging stations, large motor drives), microgrids**

State-of-the-art MV SiC Devices

- For MV SiC devices, SiC bulk resistance dominates the on-state resistance, curve closely follow SiC material 1-D limit.
- MV SiC devices are from Wolfspeed, GenSiC, USCi and Fuji.



Summary of status of SiC power devices [1]



SiC MOSFET specific on-state resistance as a function of breakdown voltage [2]

[1] F. Wang and Z. Zhang, "Overview of silicon carbide technology: device, converter, system, and application", *CPSS transaction on power electronics and applications*, vol. 1, no. 1, 2016.

[2] J W Palmour, L Cheng, V Pala, et al. Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV. *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Waikoloa, HI, USA, 15-19 June 2014.

State-of-the-art High Voltage SiC Devices

HV SiC diodes

Voltage/Current	Static	Dynamic
10kV/10A JBS diode (Wolfspeed)	4V@10A	t_{rr}=365ns, Q_{rr}=0.84μC @3.15A
10kV/50A 4H-SiC PiN (Wolfspeed)	3.9V@50A, 5.9V@328A	t_{rr}=200ns, di/dt=330kA/s @10kV/20A
12.9kV SiC PiN diode (GeneSiC)	3.3mΩ-cm^2 @25°C	NA
10kV SiC PiN diode (GeneSiC)	5.75mΩ-cm^2 @25°C	t_{rr}=250ns, Q_{rr}=1.67μC @ 2.4kV/24A
10kV/2A SiC JBS diode (GeneSiC)	114.7mΩ-cm^2 @25°C	NA
10kV/7A SiC JBS diode (GeneSiC)	127.5mΩ-cm^2 @25°C	NA
6.5kV/15A SiC JBS diode (USCi)	3.8V	NA
8kV/5A SiC JBS diode (USCi)	4.0V	NA

HV SiC bipolar devices (IGBT, IGCT, and thyristor)

Voltage/Current	Static	Dynamic
12kV/0.5A p-IGBT (Wolfspeed)	18.6mΩ-cm^2 @25°C	t_{on}=40ns, t_{off}=2.8μs @1.5kV/0.55A
12.5kV/35A n-IGBT (Wolfspeed)	5.3mΩ-cm^2 @32A,25°C	t_{off}=0.65μs @5kV/5A, 25°C
15kV/20A p-IGBT (Wolfspeed)	6.5V@20A,25 °C	NA
15kV/20A n-IGBT (Wolfspeed)	7.0V@20A,25 °C	NA
16kV flip-type n-IGBT (Fuji)	6.5V@20A	NA
22.6kV/20A n-IGBT (Wolfspeed)	NA	NA
10kV/8A BJT (GeneSiC)	110mΩ-cm^2	E_{on}=4.2mJ, E_{off}=1.6mJ @5kV/8A
6.5kV Thyristor (GeneSiC)	2.8mΩ-cm^2	dv/dt=1920 V/μs @3.6kV/14.5A

State-of-the-art MV SiC Devices

HV SiC unipolar devices (MOSFET and JFET)

Voltage/Current	Static	Dynamic
10kV/5A DMOSFET (Wolfspeed)	111mΩ-cm^2 @V_{gs}=15V,25°C	E_{on}=240μJ, E_{off}=50μJ @1.0kV/3A,25°C
6.5kV/30A Gen-3 MOSFET (Wolfspeed)	100mΩ-cm^2@25°C	NA
10kV/10A MOSFET (Wolfspeed)	127mΩ-cm^2 @V_{gs}=20V,25°C	E_{on}=4.48mJ, E_{off}=0.81mJ @5.3kV/10A
10kV/20A Gen-3 MOSFET (Wolfspeed)	86mΩ-cm^2 @V_{gs}=20V	E_{on}=6.5mJ, E_{off}=1mJ @6kV/20A
15kV/10A Gen-3 MOSFET (Wolfspeed)	208mΩ-cm^2 @V_{gs}=20V	E_{on}=4.8mJ, E_{off}=1mJ @6kV/10A
6.5kV/15A normally-off JFET (USCi)	350mΩ@25°C	E_{on}=2.71mJ, E_{off}=1.54mJ @3kV/11A
6.5kV super cascode JFET (USCi)	230mΩ@25°C	E_{on}=1.2mJ, E_{off}=0.53mJ @3kV/11A
10kV/240A MOSFET half-bridge module (Wolfspeed)	19.4mΩ	NA
6.5kV/60A JFET half-bridge module (USCi)	100mΩ@25°C	E_{on}=28mJ, E_{off}=9.2mJ @3kV/60A,25°C

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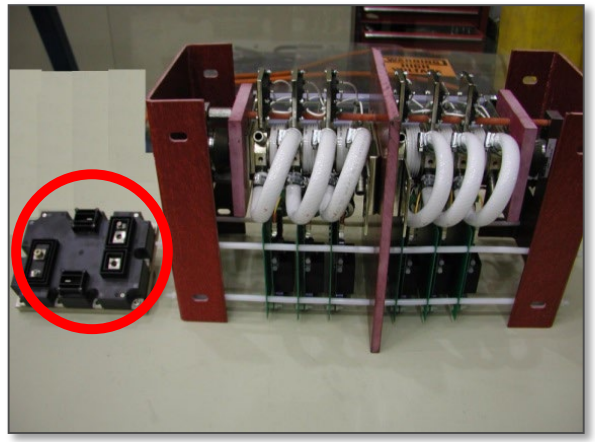
SiC Device Applications

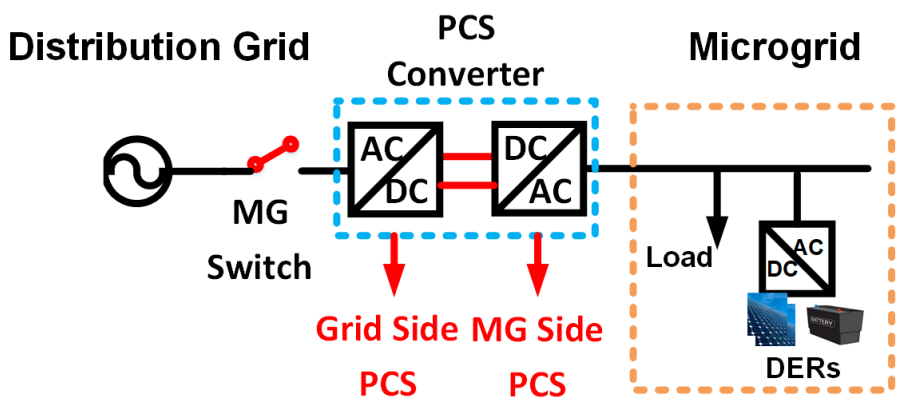
- **Silicon Carbide vs. Silicon**
  - High breakdown electric field, high voltage rating, low conduction loss
  - Fast switching speed, high switching frequency
  - Superior thermal characteristics
- **Applications should take advantages of**
  - Low loss
  - Fast switching speed
  - High frequency application
- **Benefits of MV SiC can be realized in several ways**
  - Direct substitution – improved efficiency and power density
  - Simplified topology/converter – further loss reduction, increased power density, better reliability
  - Enable new capability and functionality for system-level (e.g. smart inverters)
  - Enable new applications or replace the non-PE equipment (e.g., SST, DC grid)

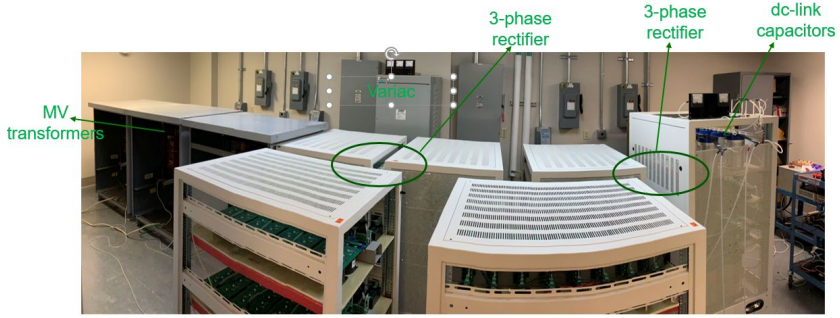
SiC vs. Silicon
1MW Comparison of Switches



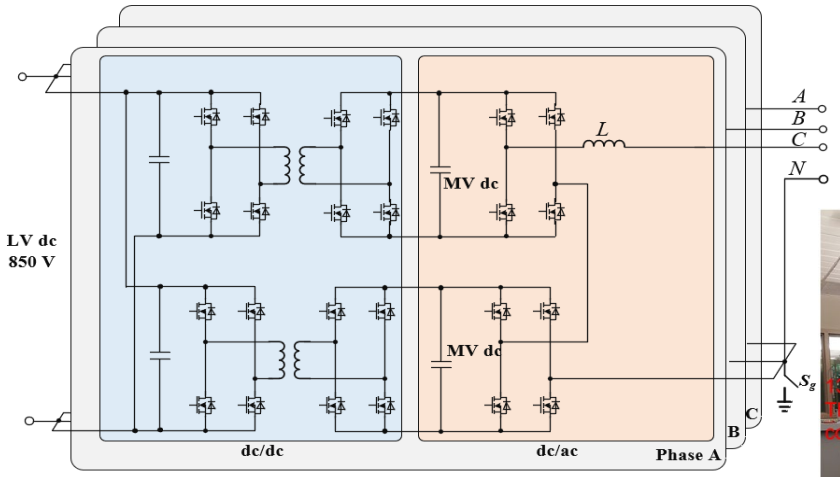
Wolfspeed 10 kV/240A SiC MOSFET

Recent SiC MV Grid-tied Power Converters

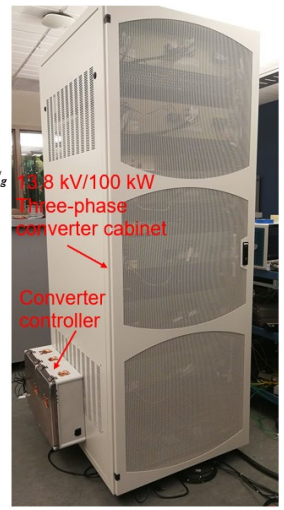


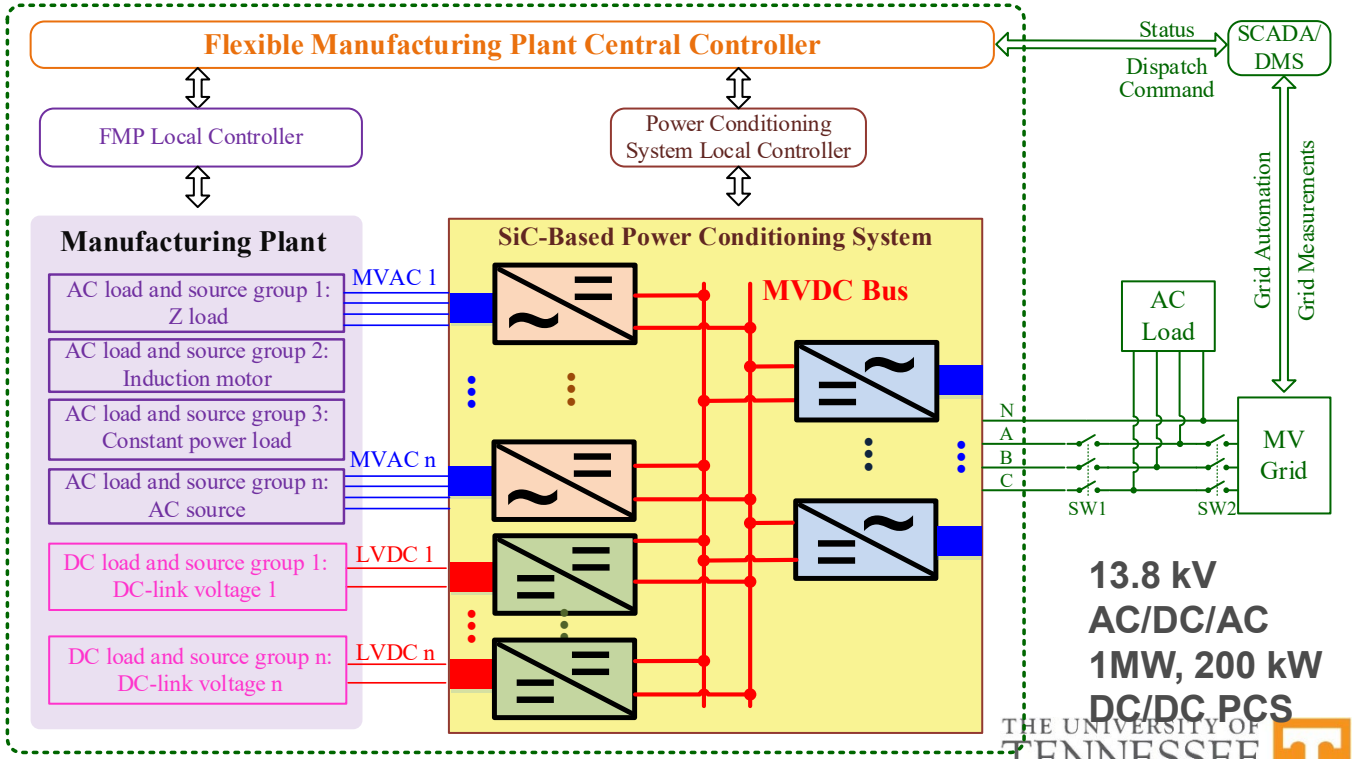


13.8 kV AC/DC/AC power conditioning system(PCS) prototype



13.8 kV AC/850 V DC PCS for flexible CHP

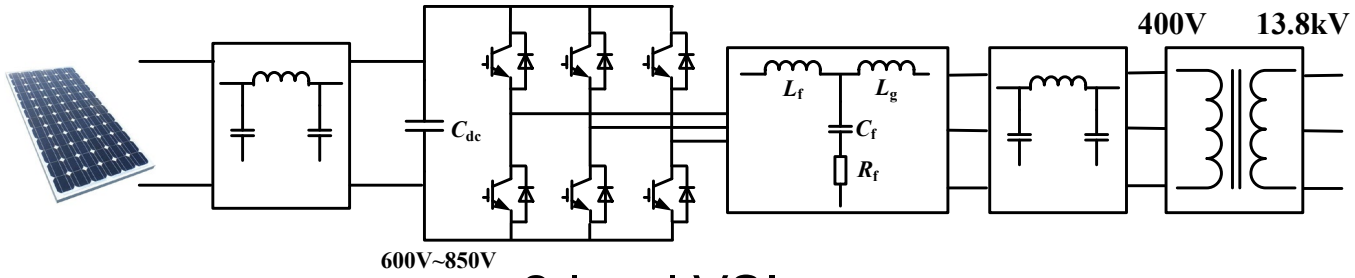




13.8 kV AC/DC/AC 1MW, 200 kW DC/DC PCS

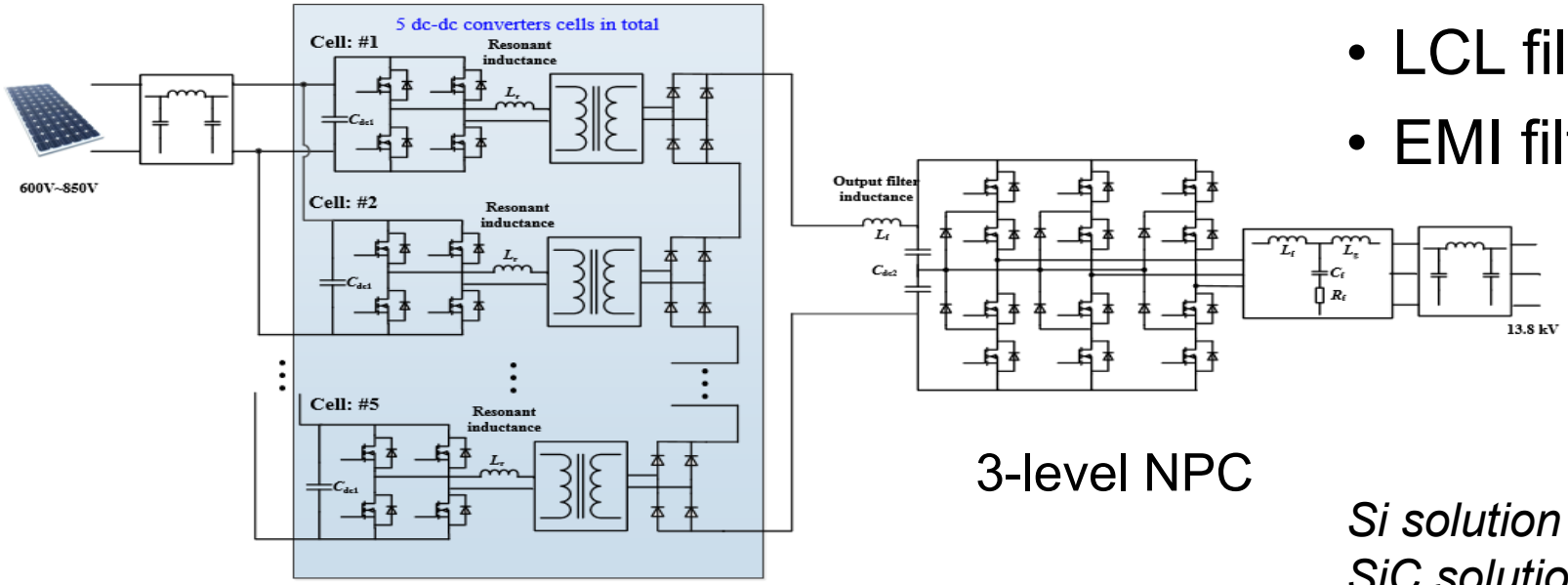
SiC PV Converter Benefits in MV AC Grids – Converter Level

Si-Based PV converter



2-level VSI

SiC-Based PV converter



PSFB

3-level NPC

- Converter topology
  - ❑ Si-based: 2-level
  - ❑ SiC-based: 3-level NPC & PSFB
- Transformer
  - ❑ Si-based: LF transformer
  - ❑ SiC-based: HF transformer
- LCL filter
- EMI filter

Si solution based on a commercial product
SiC solution based on an ARPA-e project

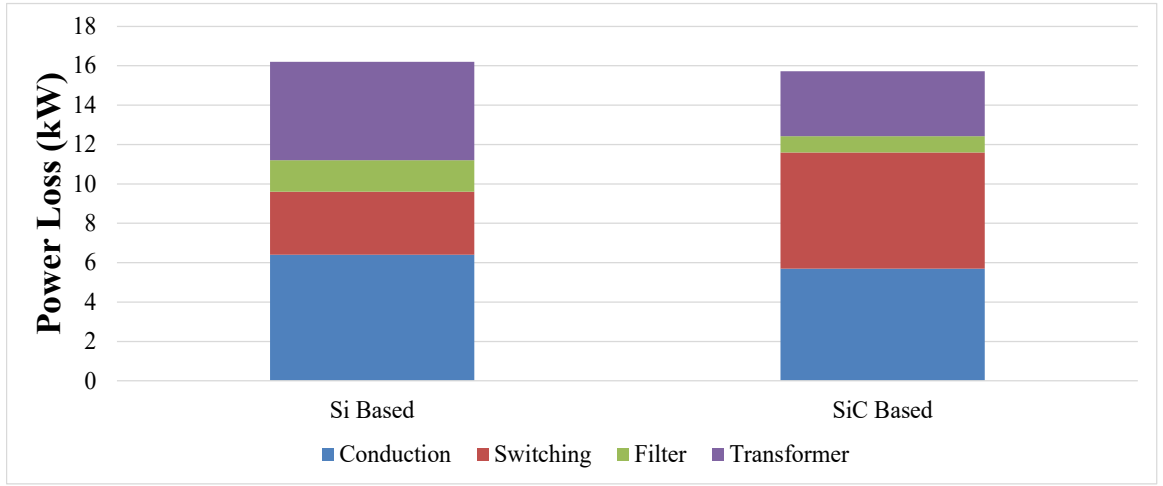
Specifications of the PV Converter

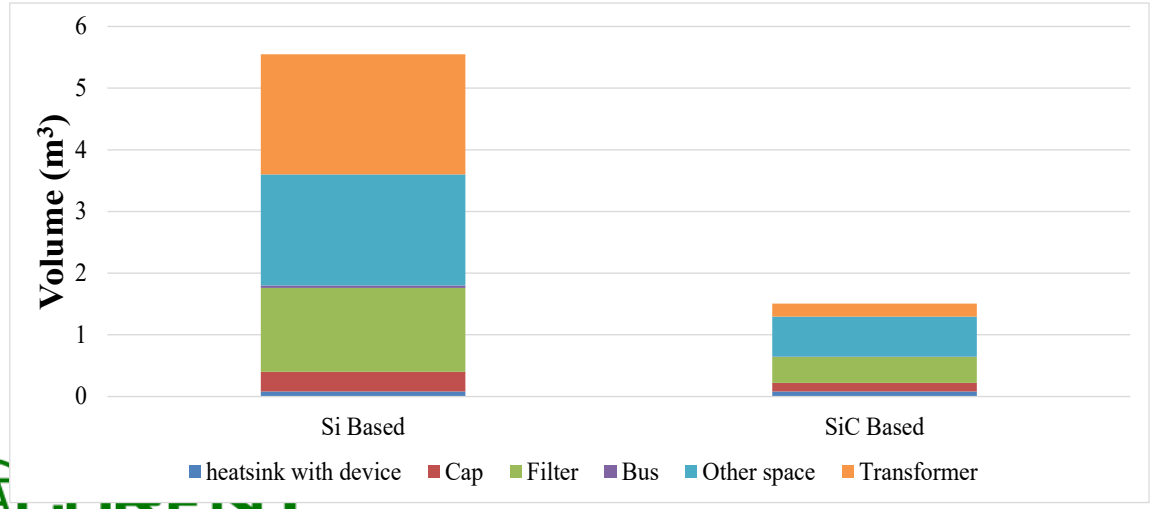
Specifications (for Si and SiC)			
Input (DC)			
Maximum input power	1.2 MW	Maximum DC current	1.71 kA
DC voltage	600 V~850 V	Maximum DC voltage	1.1 kV
DC ripple current	Not given		
Output (Three-phase AC)			
Nominal output power	1 MW	Maximum output power	1.2 MW
Nominal AC voltage	400 V (±10%) (Si) 13.8 kV (±10%) (SiC)	Nominal/Max AC current	1,519 A (Si) 44 A (SiC)
EMC	FCC 15 CLASS B	THD	<3%
Max Efficiency (1)	98.8%	Power Factor	0.95
Grid functions	Reactive power compensation, power curtailment, low voltage ride-through (LVRT)		
Ambient temp range	-15 °C~55 °C	Cooling	Forced Air

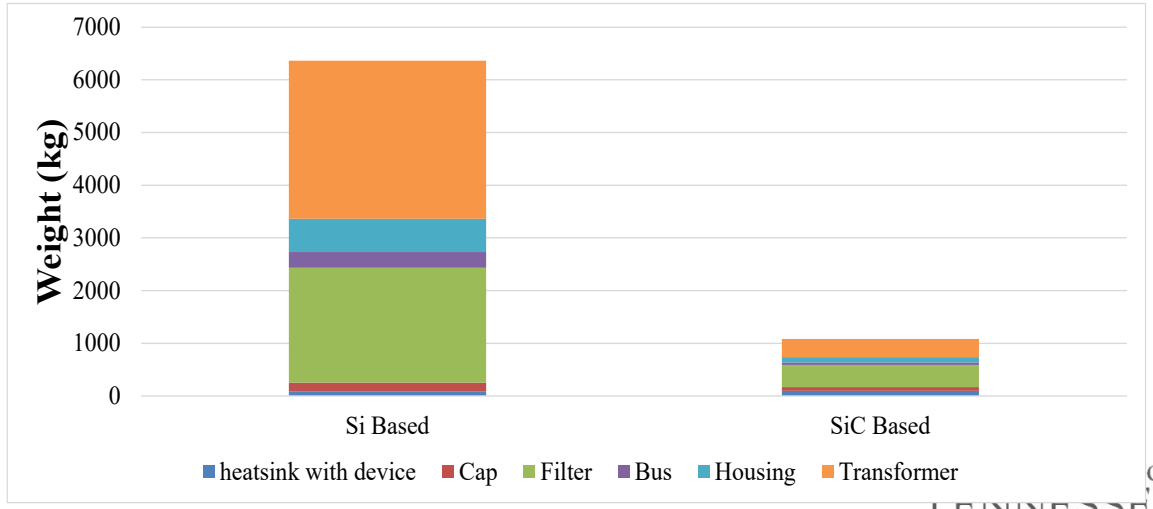
(1) Without auxiliary power consumption at min V_{DC}

Summary of Converter Design Comparison

- As expected, SiC based MV MW PV inverters can be significantly smaller (73.2%) and lighter (82.9%) than Si counterparts, and can translate into significant cost benefit in future
- Similar design comparison can be extended to BESS converters and other interface converters

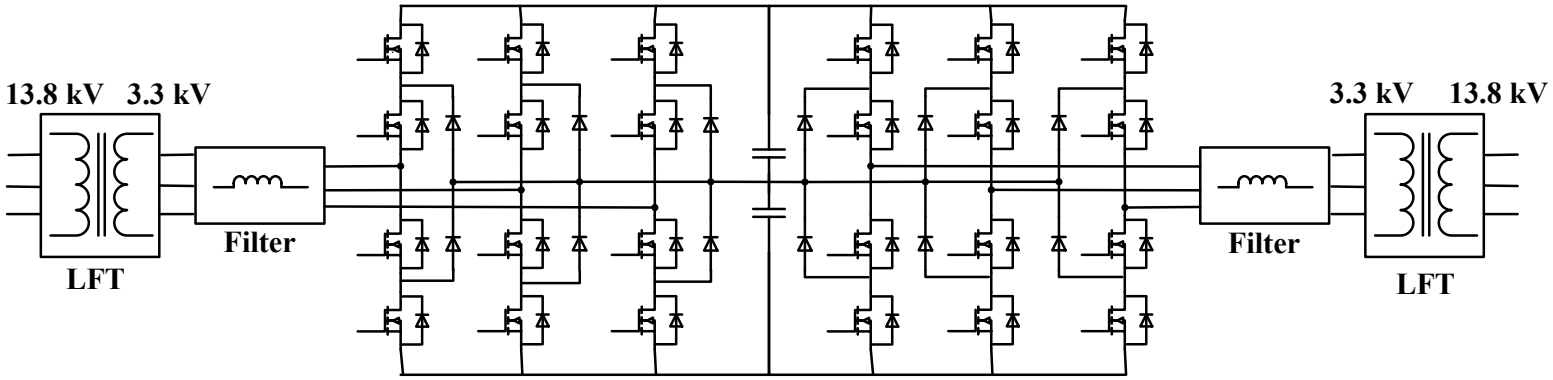






SiC PCS Benefits – Converter Level

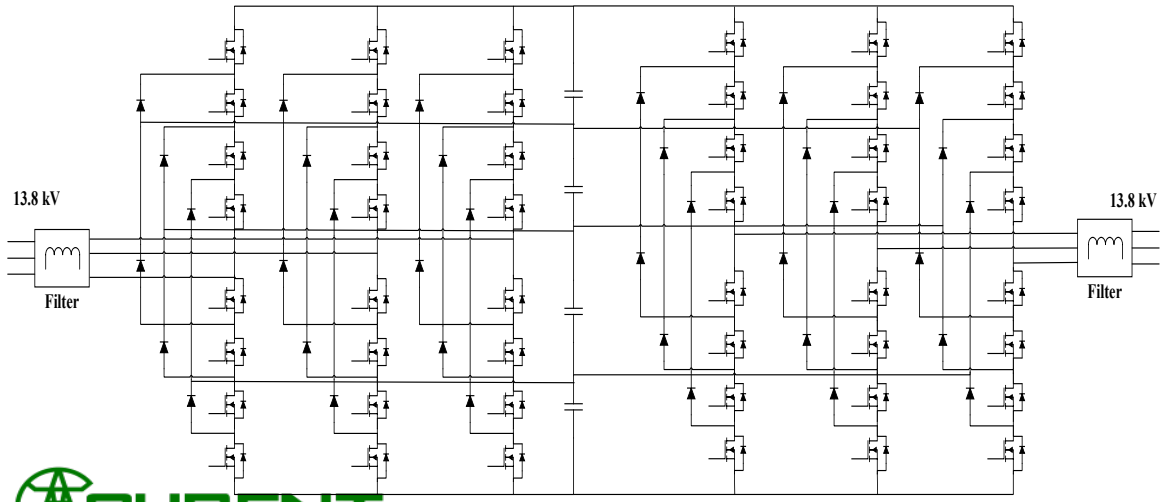
❑ Si-Based PCS converter: 3-level NPC



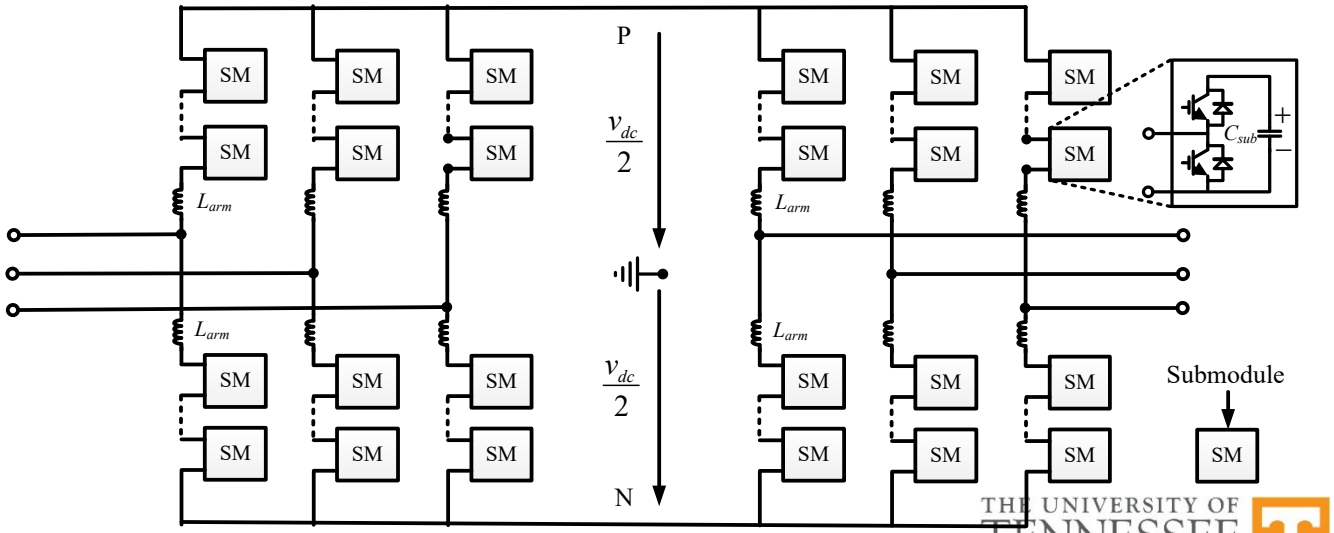
Si solution based on a commercial solution

- Converter topologies:
  - Si-based: 3-level NPC
  - SiC-based 1: 5-level NPC
  - SiC-based 2: MMC
- Transformer
  - Si-based: LF transformer
- Output filter

❑ SiC-Based PCS converter 1: 5-level NPC



❑ SiC-Based PCS converter 2: MMC



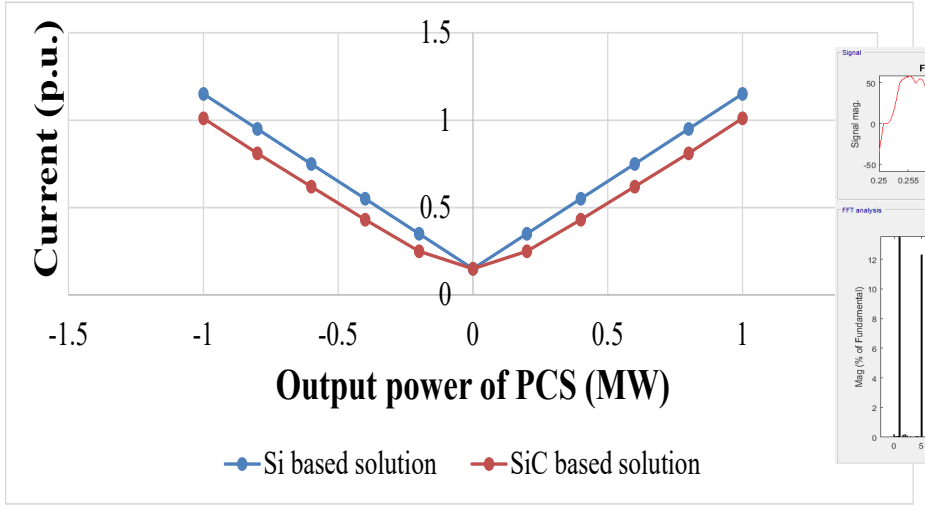
Comparison Summary

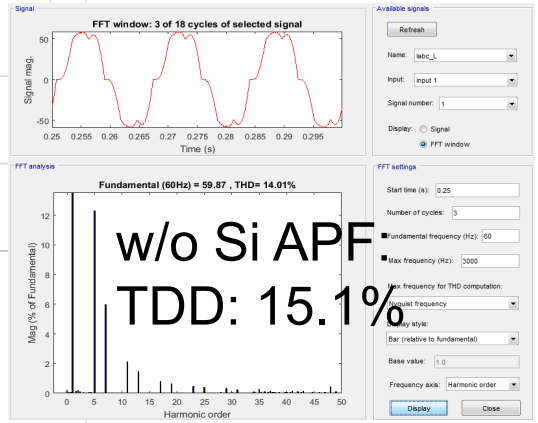
- SiC-based MV MW PCS converter can be significantly smaller than Si counterparts
  - Weight: SiC-based NPC and MMC save 98% and 92% compared to Si
  - Size: SiC-based NPC and MMC save 98% and 86% compared to Si
  - Efficiency of Si-based NPC is 98.52% @1 kHz, similar to SiC-based NPC 98.6% @20 kHz and MMC 98.6% @10 kHz

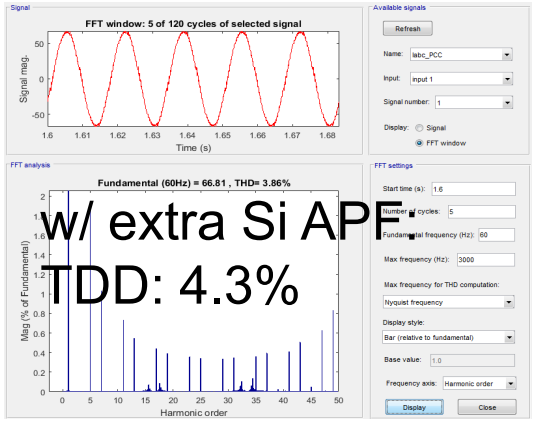
	Weight (kg)				Size (m^3)			
	Si- NPC	SiC- NPC 10 kHz	SiC- NPC 20 kHz	SiC- MMC	Si- NPC	SiC- NPC 10 kHz	SiC- NPC 20 kHz	SiC- MMC
Device w/ heatsink	164 kg	43 kg	43 kg	35 kg	0.14 m^3	0.017 m^3	0.017 m^3	0.014 m^3
Inductor	2,700 kg	45 kg	32 kg	143 kg	2.32 m^3	0.016 m^3	0.011 m^3	0.066 m^3
Capacitor	158 kg	26 kg	13 kg	429 kg	0.1 m^3	0.036 m^3	0.018 m^3	0.58 m^3
Busbar	73 kg	9.2 kg	9.2 kg	12 kg	0.008 m^3	0.002 m^3	0.002 m^3	0.002 m^3
Housing	344 kg	13.7 kg	11 kg	69 kg	-	-	-	-
Transformer	5,600 kg	-	-	-	4.12 m^3	-	-	-
Total	9,039 kg	137 kg	108 kg	688 kg	9.24 m^3	0.142 m^3	0.1 m^3	1.33 m^3

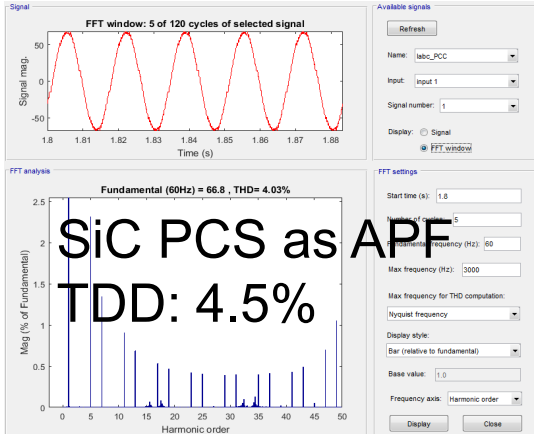
SiC PCS Converter for Enhanced Power Quality

- SiC-based PCS, with sufficient control bandwidth, can provide harmonic filtering function
  - Need an extra 150 kVA (15% more) converter for Si-based APF
  - Impact on SiC-based converter rating is minimal (~1%)





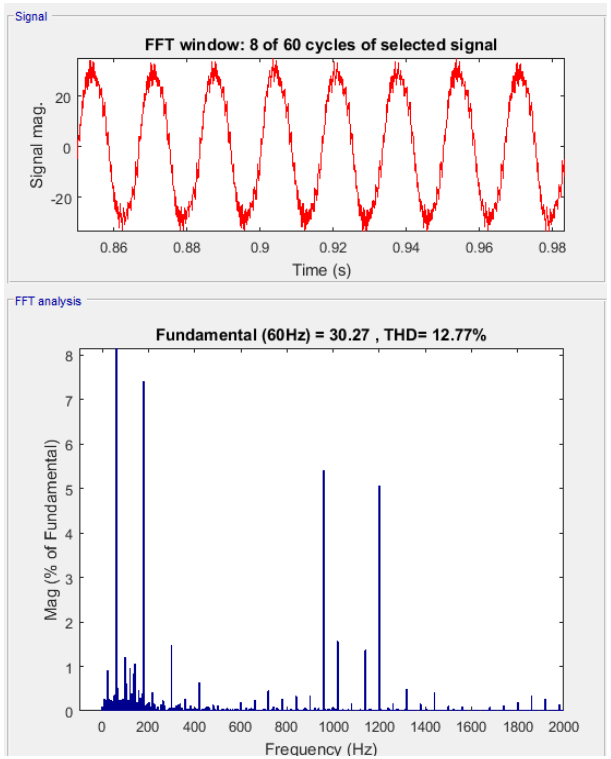




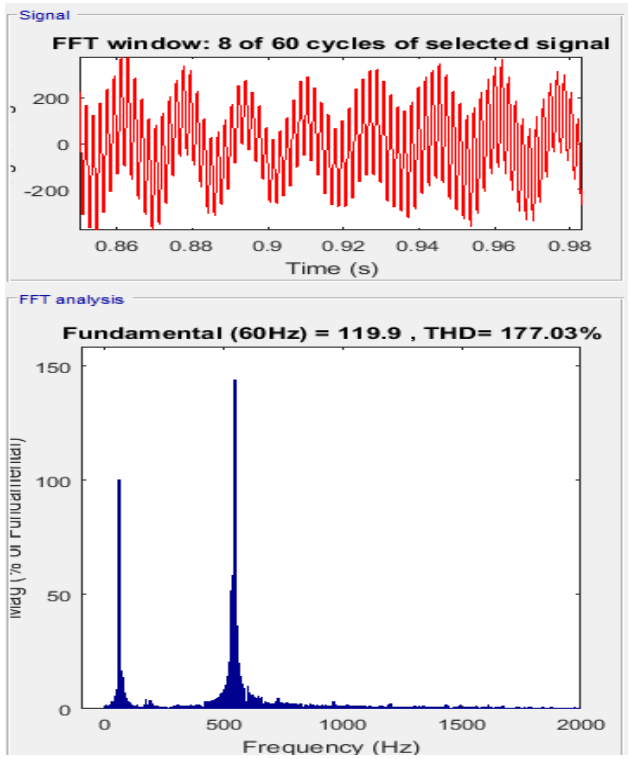
	-1 MW	-0.8	-0.6	-0.4	-0.2	0	0.2	0.4	0.6	0.8	1 MW
Si-based w/o APF	14.8% 1.001	14.9% 0.802	15.0% 0.602	15.0% 0.403	15.1% 0.206	15.1% 0.045	15.1% 0.206	15.2% 0.403	15.2% 0.602	15.3% 0.802	15.3% 1.001
Si-based w/ APF	4.1% 1.15	4.5% 0.95	4.2% 0.75	4.3% 0.55	4.2% 0.35	4.3% 0.15	4.2% 0.35	4.4% 0.55	4.1% 0.75	4.3% 0.95	4.2% 1.15
SiC-based	4.5% 1.01	4.3% 0.81	4.1% 0.62	4.2% 0.43	4.3% 0.25	4.5% 0.15	4.2% 0.25	4.4% 0.43	4.3% 0.62	4.1% 0.81	4.2% 1.01

SiC PCS Converter for Enhanced Stability

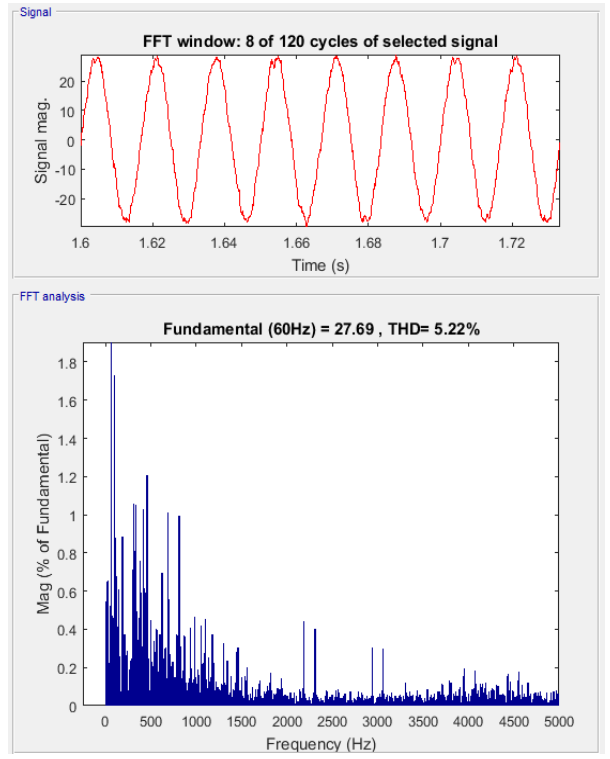
- Grid-connected mode
  - Si-based PCS: Unstable if capacitor is placed at grid side
  - SiC-based PCS: Still stable even though capacitor is placed at grid side



Grid impedance 0.05 p.u.



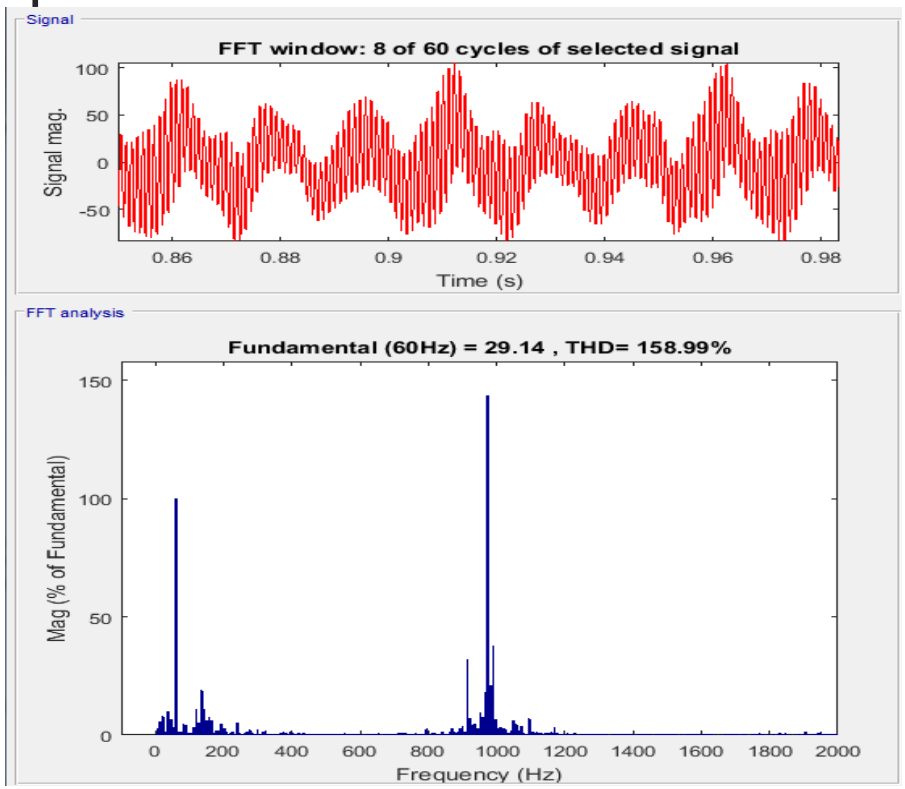
Si- PCS, Grid impedance 0.1 p.u.
PFC cap at grid side 0.163 p.u.



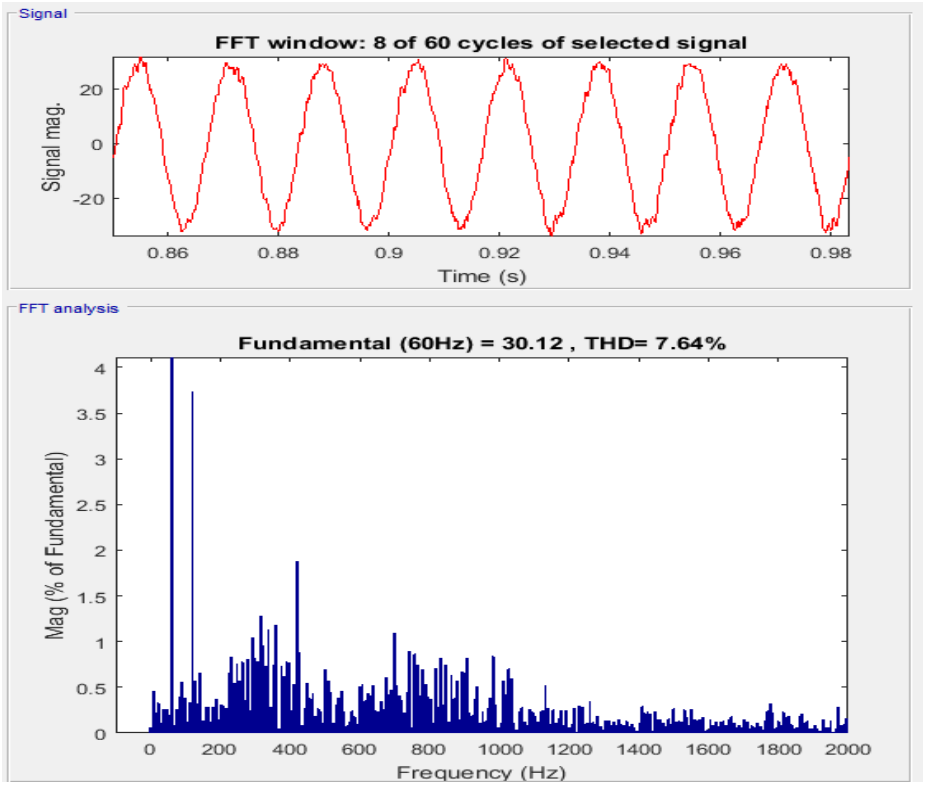
SiC- PCS, Grid impedance 0.1 p.u.
PFC cap at grid side 0.163 p.u.

SiC PCS Converter for Enhanced Stability

- Islanded mode
  - Si-based PCS: Unstable with heavy capacitive load and multiple RESs
  - SiC-based PCS: Still stable even though with heavy capacitive load and multiple RESs



Si-based PCS



SiC-based PCS

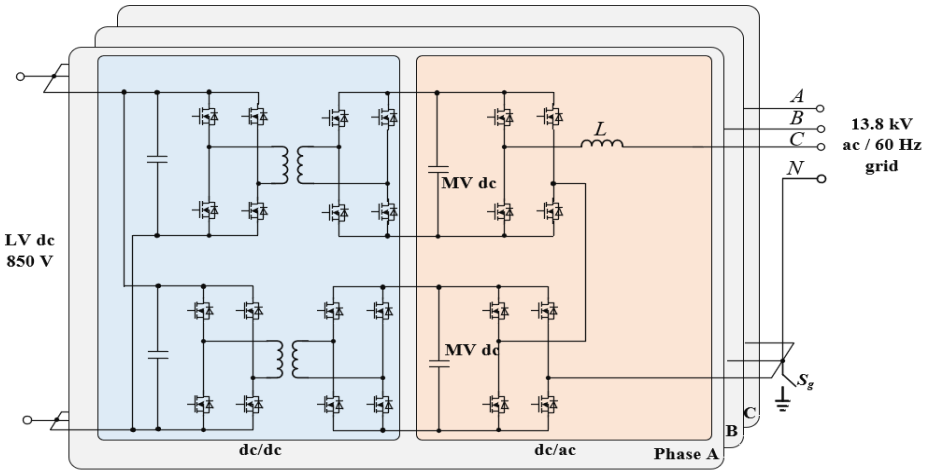
MV SiC Power Electronics Presentation Outline

- ❑ Overview
- ❑ Benefits of MV SiC Power Electronics for Grid Applications
- ❑ MV SiC Power Electronics Converter Design Considering Grid Requirements
- ❑ Some Example Design and Control Issues
- ❑ Summary

A Cascaded H-bridge-based 13.8 kV/1 MW Grid-Connected Converter Design Considering Grid Requirements

❑ Design Requirements

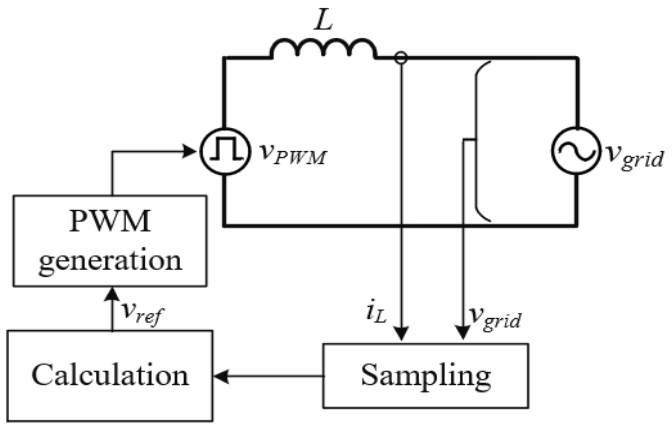
Converter design parameters	Power rating	1 MW
	LV DC	850 V (±5%)
	MV AC	13.8 kV (-12% ~ 10%)
	MV AC frequency	60 Hz (±1.2 Hz)
	Efficiency	98 %
	Power factor	Four-quadrant operation
	Ambient temperature	-25 ºC ~ 35 ºC
	Cooling	Forced air / water cooling
	Voltage control bandwidth	>300 Hz
	Current control bandwidth	>1 kHz
Grid requirements	IEEE Std 1547	▪ 5% current TDD ▪ VRT ▪ FRT
	Other requirements	▪ Grid Faults ▪ Grid unbalance operation ▪ Lightning transient ▪ 33% unbalance load support in the islanded mode



Converter topology

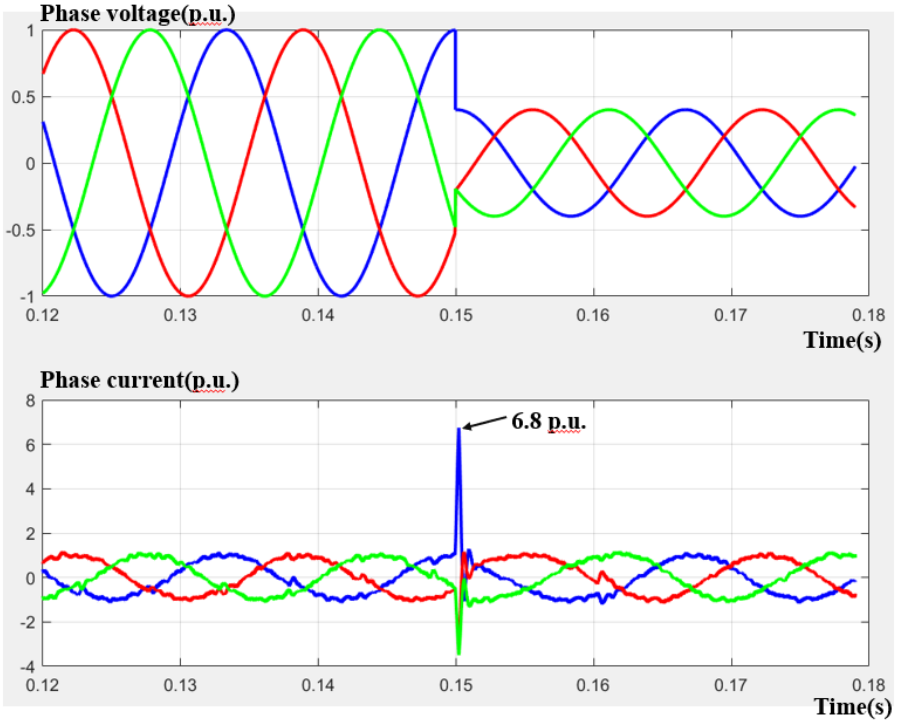
Example - Impact of Voltage Ride Through

- Design goal: continuous operation range: [0.88 p.u., 1.1 p.u.]; converter ride through [0, 0.88 p.u.] and [1.1 p.u., 1.2 p.u.]
- High inrush current and high DC link voltage during grid voltage change transient



$$\Delta i_L \approx \frac{\Delta v_{grid}}{L} T_d$$

Δi_L: inrush current
Δv_{grid}: grid voltage change amplitude
T_d: control delay time



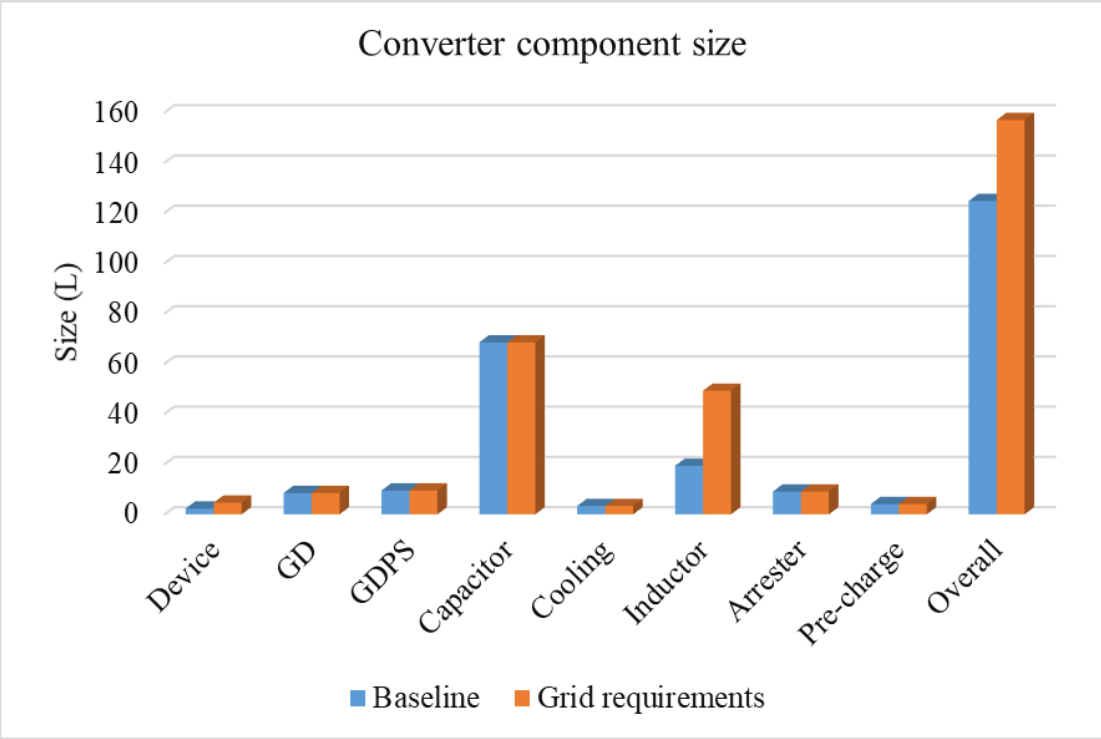
Inrush current at the transient of grid voltage change

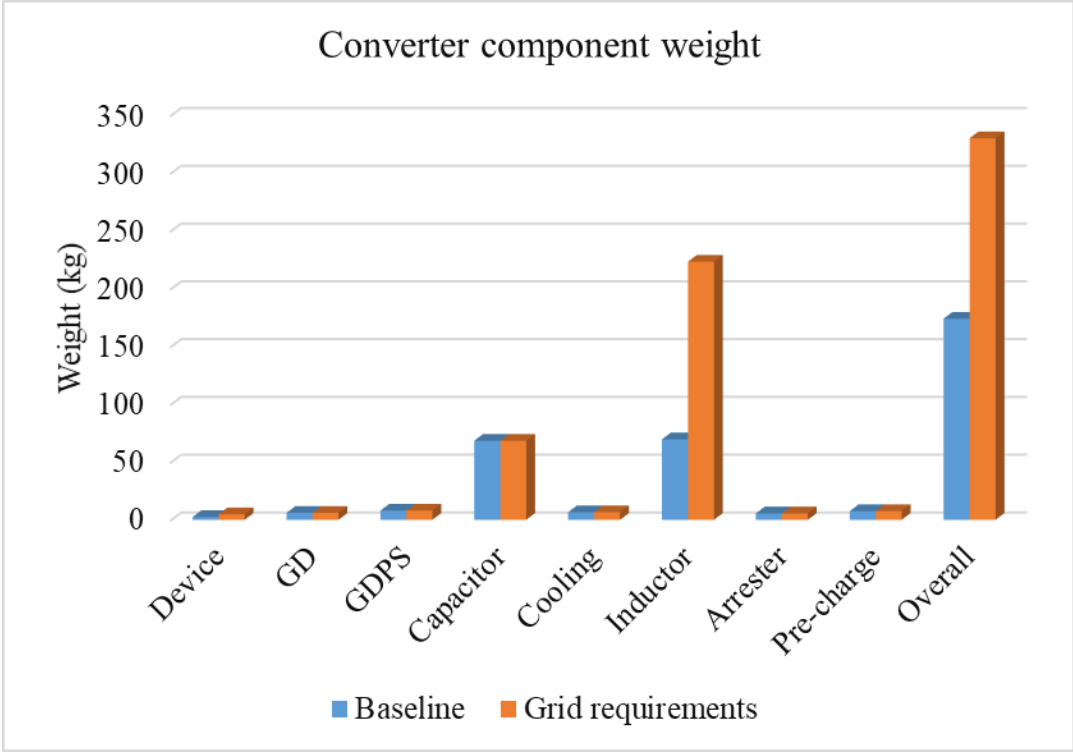
PCS Design Considering Grid Requirements

Grid/design requirements	Requirement details	Impact on converter design
Voltage ride through	• The converter needs to ride through the low voltage range of [0, 0.88 p.u.], and the high voltage range of [1.1 p.u., 1.2 p.u.]	• Inrush current, can be effectively limited by the PWM mask function • Vdc increased from 6.3 kV to 6.67 kV for 1.2 p.u. grid voltage • Power control coordination
Grid faults	• Ride through if TOV <1.2 p.u. • If TOV>1.2 p.u., temporarily stop operation	• Inrush current: up to 5 p.u. • Dc-link overvoltage, up to 9.3 kV • Extra braking circuit
Frequency ride through	• Continuous operation: [58.8 Hz, 61.2 Hz] • Ride through: [50 Hz, 58.8 Hz] and [61.2 Hz, 66 Hz]	• No inrush and large dc-link overvoltage • Need larger dc-link capacitance to limit the dc-link voltage ripple
Grid voltage angle change	• Ride through 20º of positive-sequence phase angle change and up to 60º of individual phase angle change	• Inrush current, but can be effectively limited by the PWM mask function • Dc-link voltage variation, but no need for hardware change
Lightning surge	• Ride through the lightning surge	• Inrush current, up to 5 p.u. • Dc-link overvoltage, which is not too large thanks to the short period • Converter internal component insulation need to consider the potential of the neutral point during the lightning transient

Impact on Converter Size and Weight

- Size increases 26% (commercial capacitors are used, so DC-link capacitor impact is not reflected)
- Weight increases 90%





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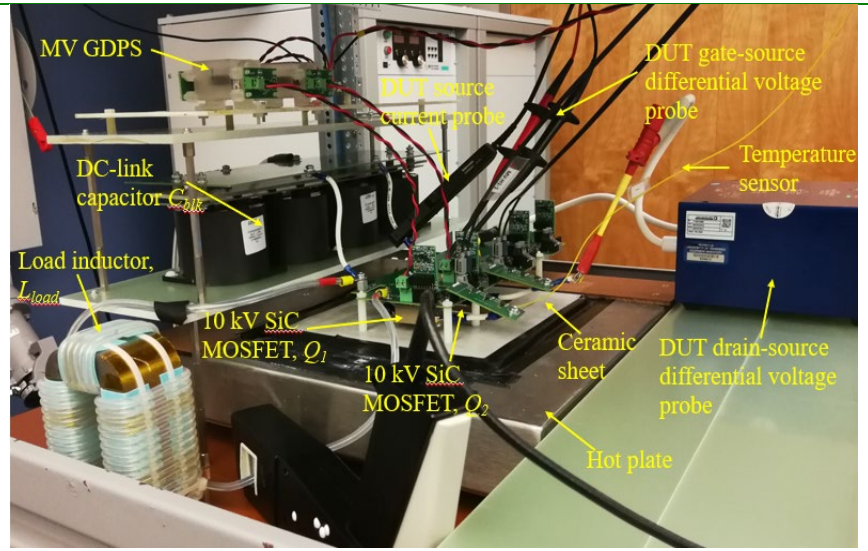
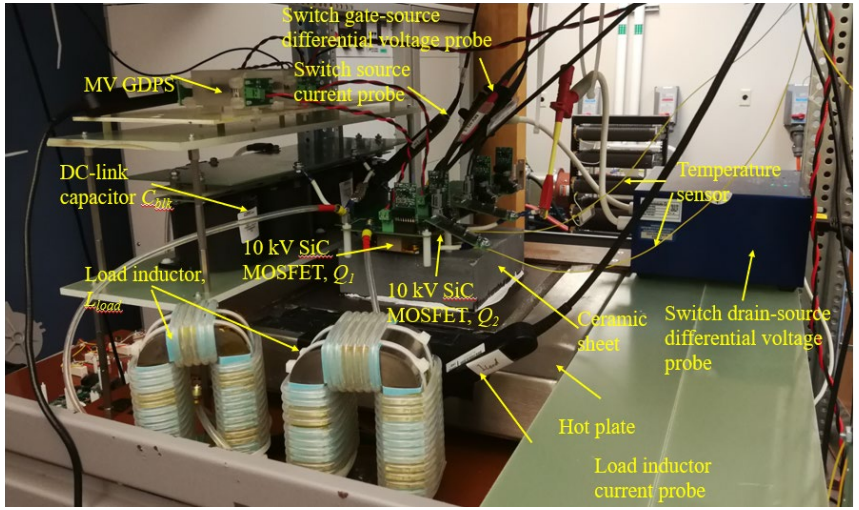
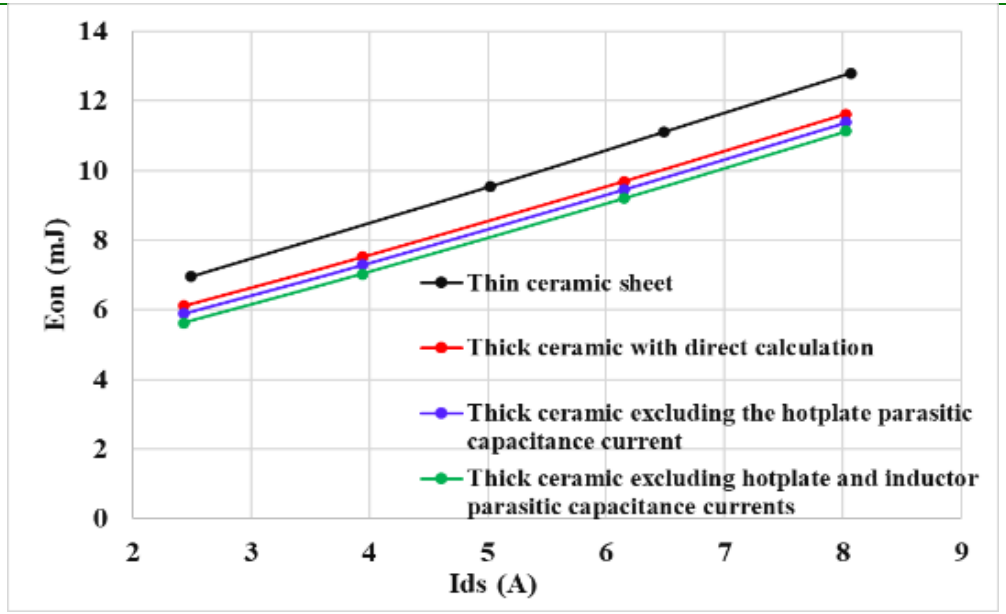
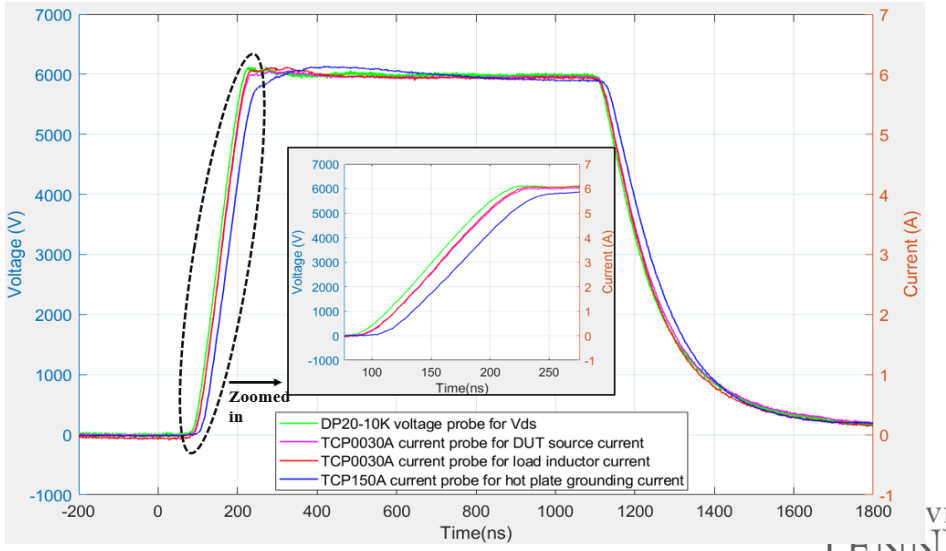
10 kV SiC MOSFET Characterization







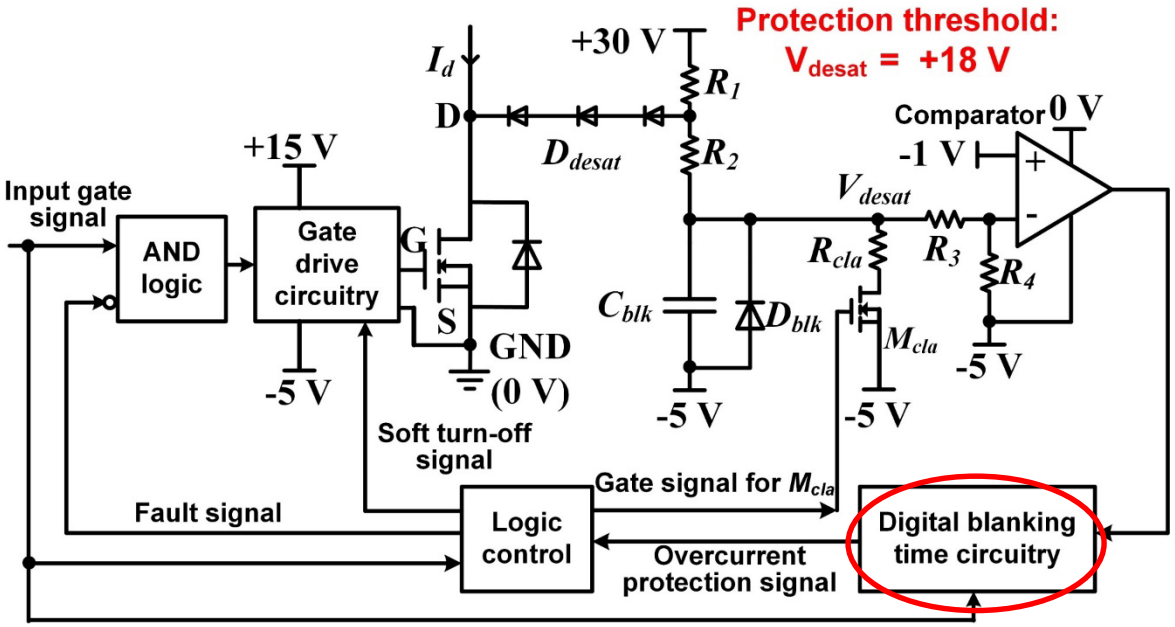


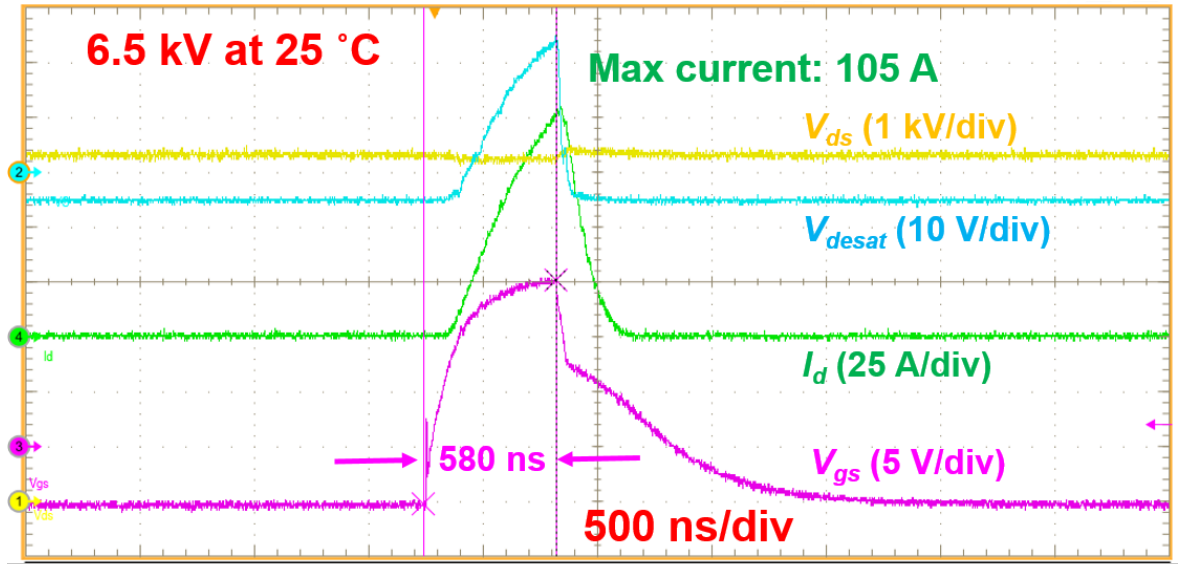
[1] Li et al "Improved Double Pulse Test for Accurate Dynamic Characterization of Medium Voltage SiC Devices," *IEEE Transactions on Power Electronics,* 2023

Gate Driver Design and Protection

- 550 ns blanking time required to avoid false triggering
- 600 ns blanking time realized by digital ICs, instead of a large blanking capacitor Cblk

- Short circuit inductance under HSF fault: 171 nH
- Measured digital blanking time: 580 ns
- Response time under HSF fault: 340 ns
- Response time under FUL fault: 195 ns



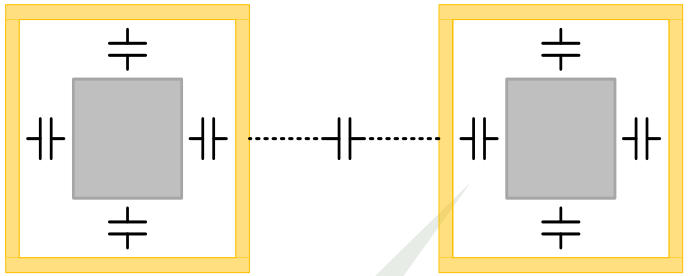


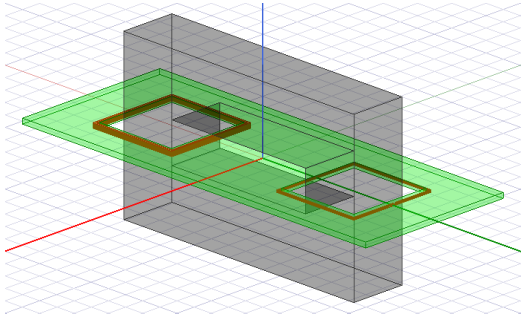
[1] X. Huang et al., "Comprehensive Analysis and Improvement Methods of Noise Immunity of Desat Protection for High Voltage SiC MOSFETs With High DV/DT," in IEEE Open Journal of Power Electronics, vol. 3, pp. 36-50, 2022.

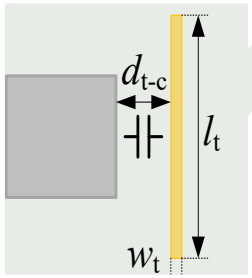
High Voltage Isolated Power Supply

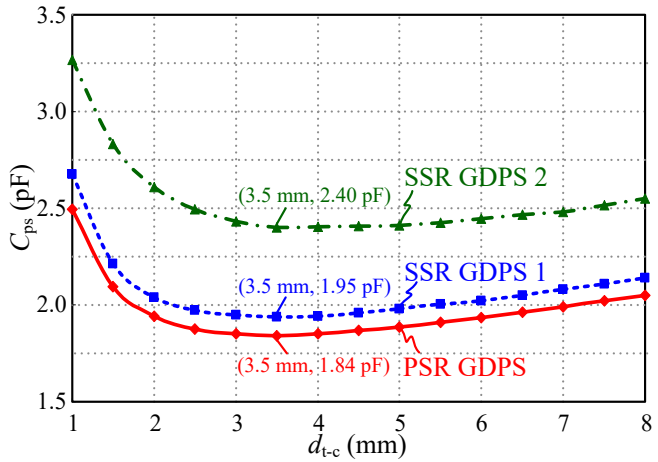
❑Low-Interwinding Capacitance Design

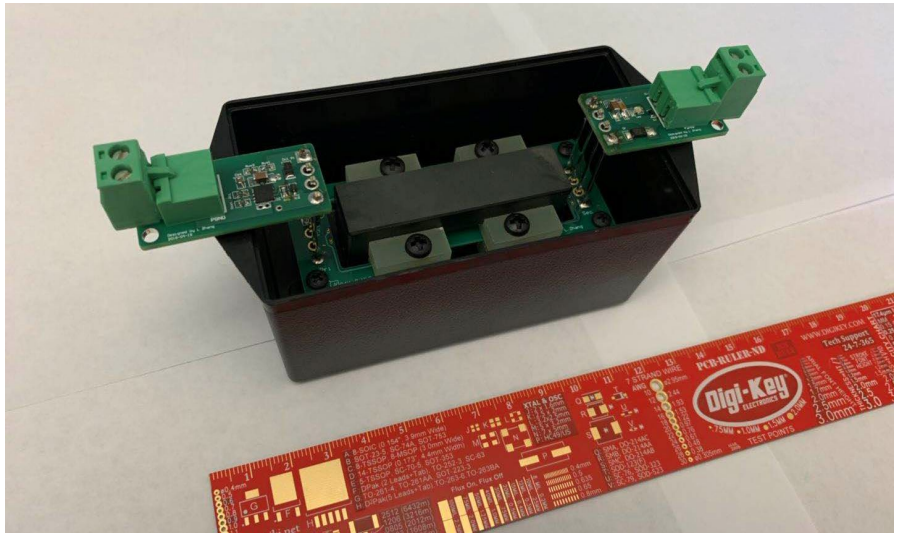
- Reduce the trace's width-to-thickness ratio
- Choose the optimal winding-to-core distance
- Reduce winding turns







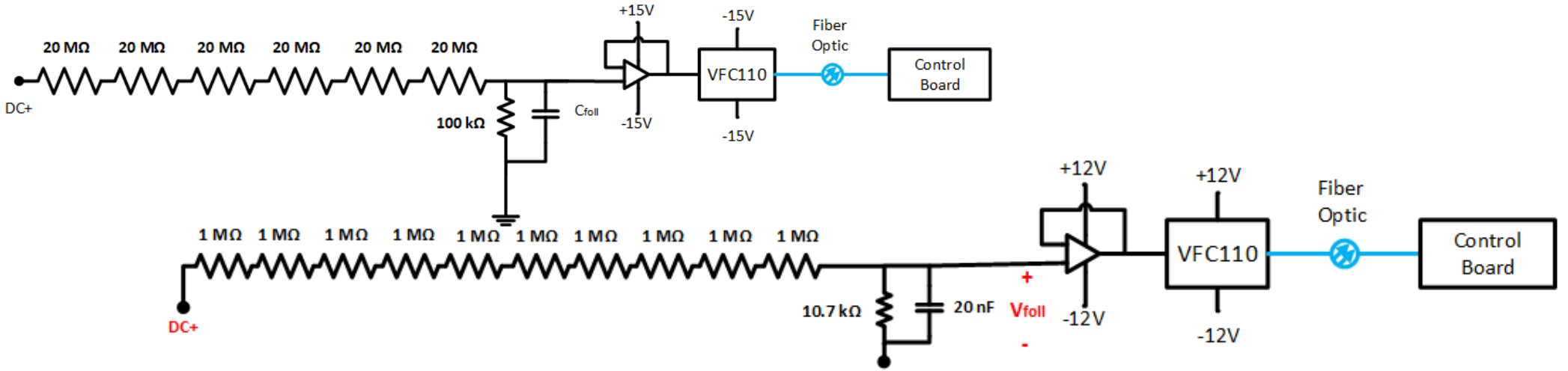


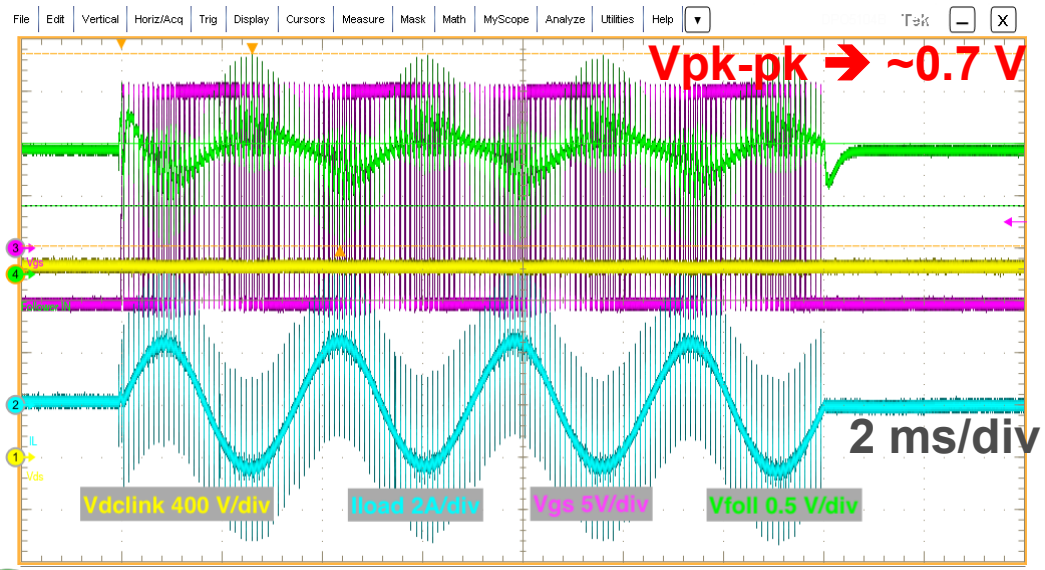


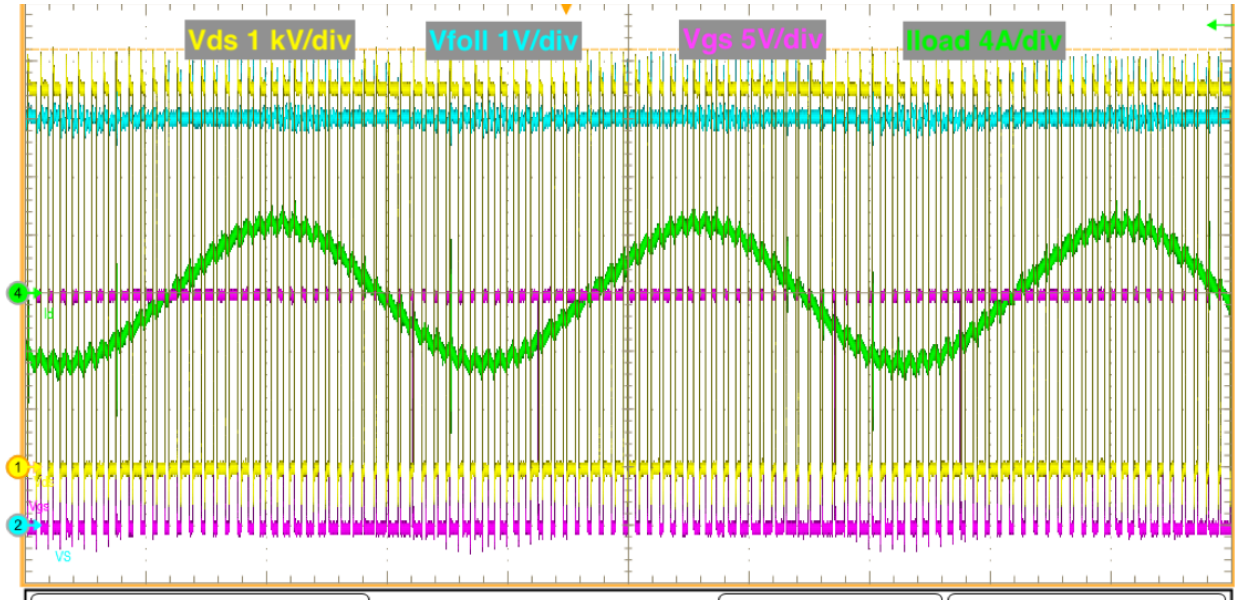
- ~1.85 pF parasitic capacitance
- >15 kV RMS partial discharge inception voltage

[1] L. Zhang et al., "Design Considerations for High-Voltage Insulated Gate Drive Power Supply for 10-kV SiC MOSFET Applied in Medium-Voltage Converter," *in IEEE Transactions on Industrial Electronics*, vol. 68, no. 7, pp. 5712-5724, July 2021.

Voltage Sensor

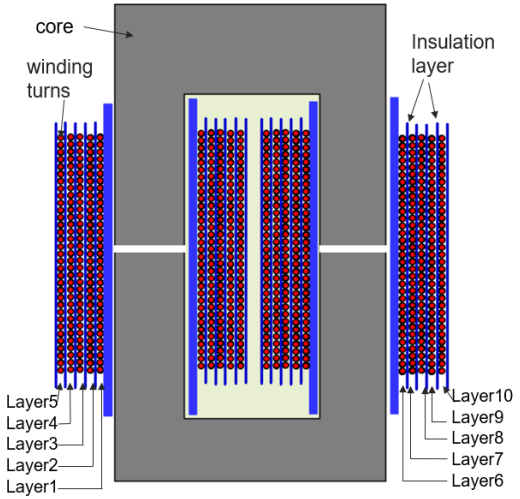


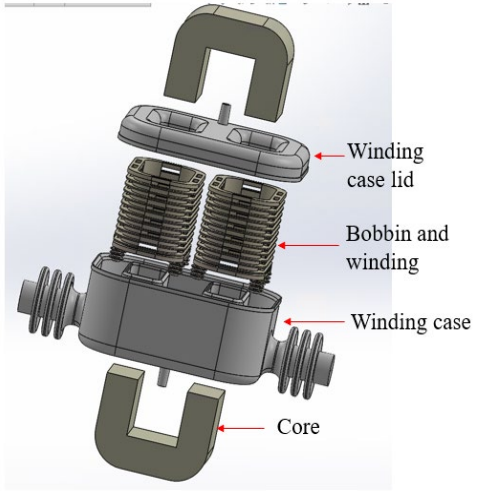


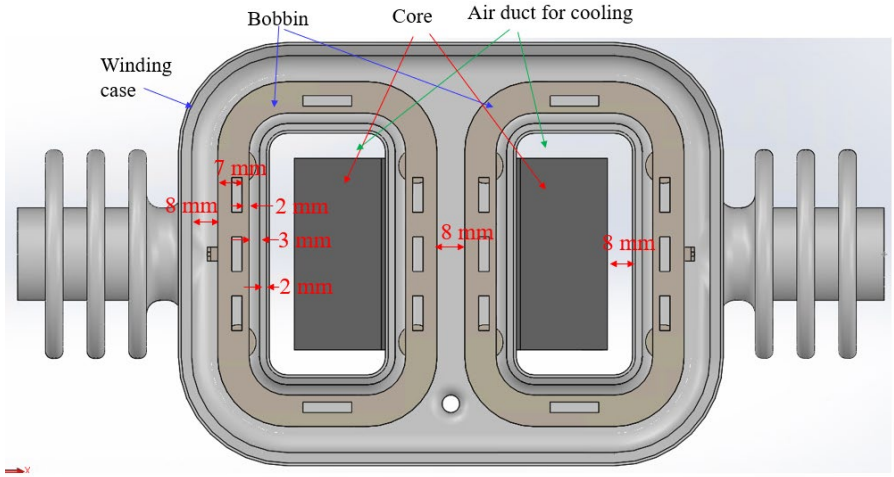


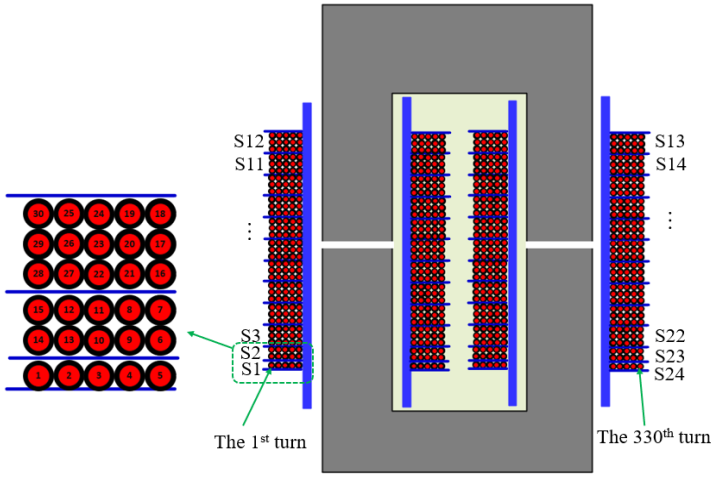
[1] J. Palmer et al., "Improving Voltage Sensor Noise Immunity in a High Voltage and High dv/dt Environment," *APEC*, 2020.

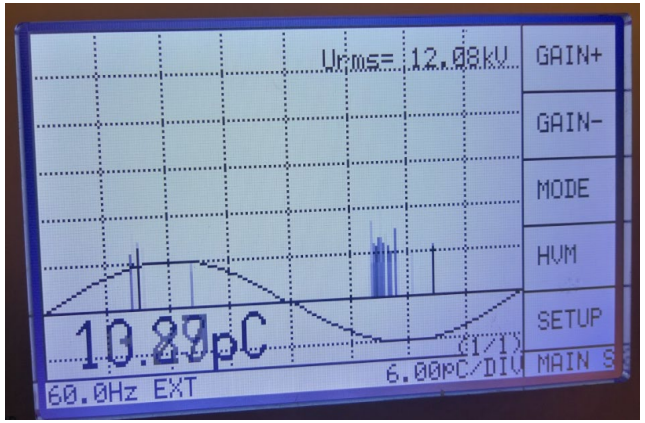
MV Inductor Design Considering Grid Overvoltages

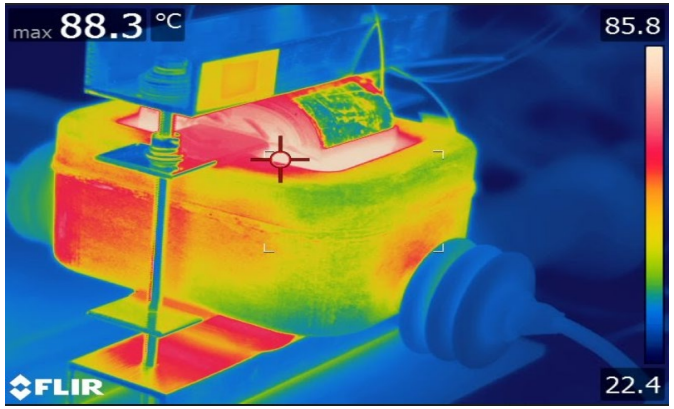










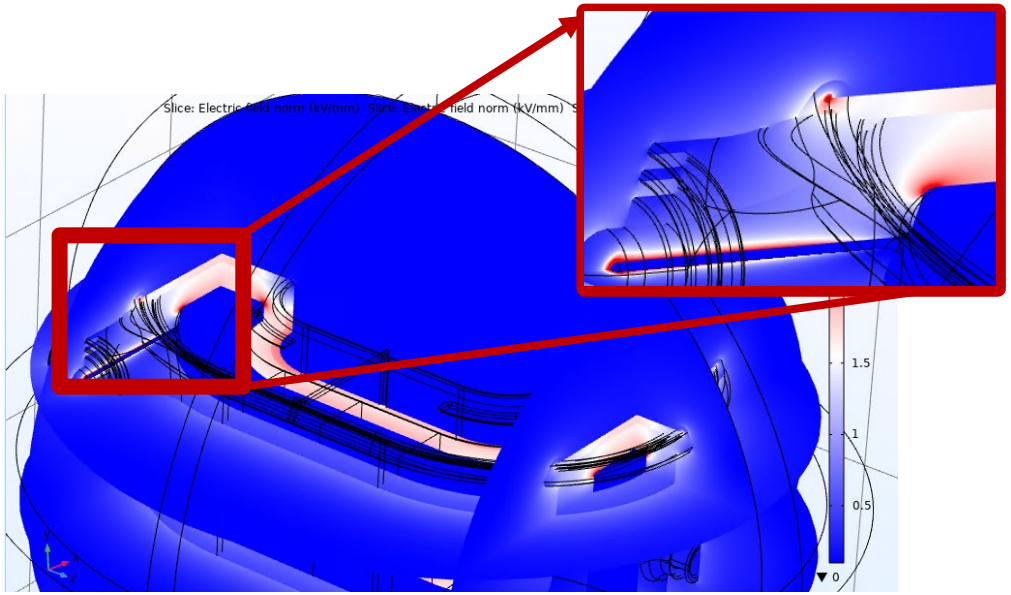


[1] H. Li, P. Yao, Z. Gao and F. Wang, "Medium Voltage Converter Inductor Insulation Design Considering Grid Requirements," *IEEE JESTPE*, Vol. 10, No. 2 2022

Insulation for MV Inductors & Transformers

- Impurity and voids in potting process caused insulation failure
- Low viscosity potting material & modified potting process used for high insulation
- Field shaping w/ silicone putty to further reduce electric field hot spot
- Transformers tested complying to IEEE Std. C57.12.91-2020. (PDIV > 12 kVrms)

Failed Dry-type MV winding

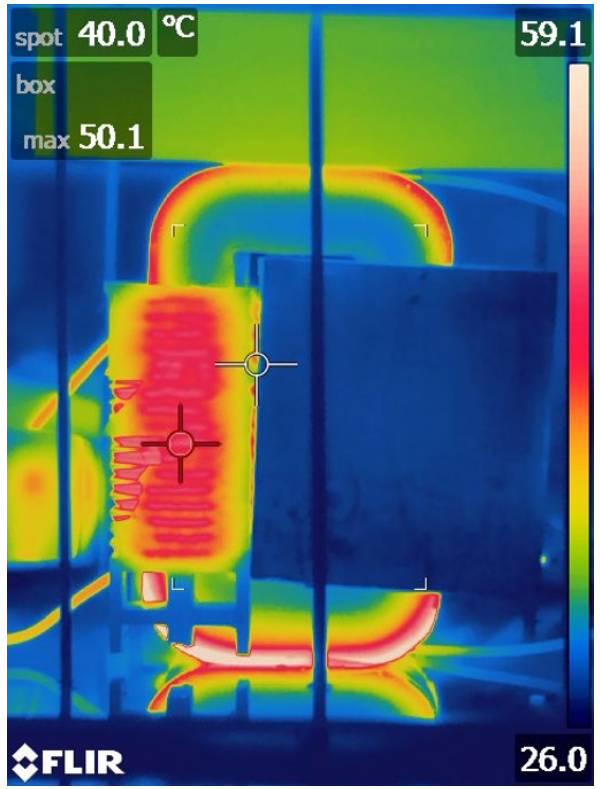


Electric field w/ fielding shaping

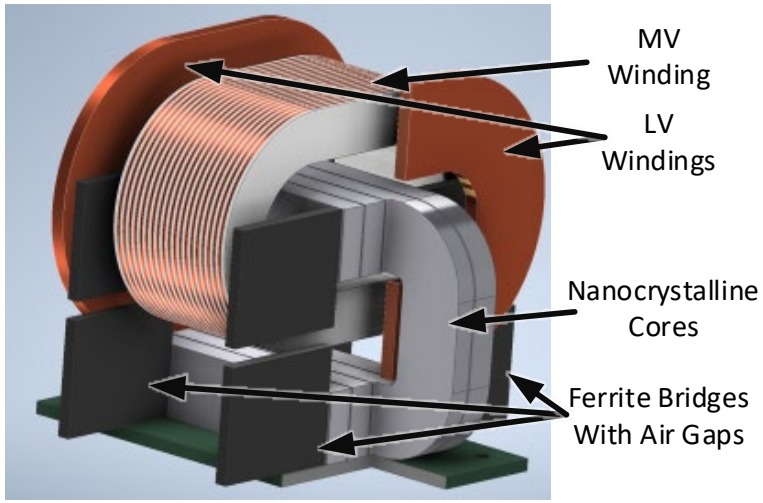
[1] H. Li, P. Yao, Z. Gao and F. Wang, "Medium Voltage Converter Inductor Insulation Design Considering Grid Requirements," *IEEE JESTPE*, Vol. 10, No. 2 2022

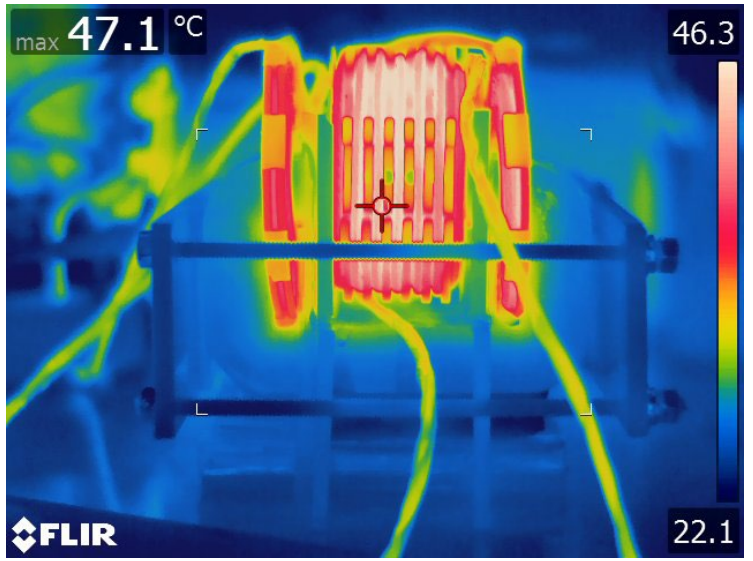
Transformer Leakage Inductance Integration

- Leakage integration caused high loss due to eddy current on core lamination
- Ferrite bridge-based transformer leakage integration reduced the loss



Thermal image of eddy current loss



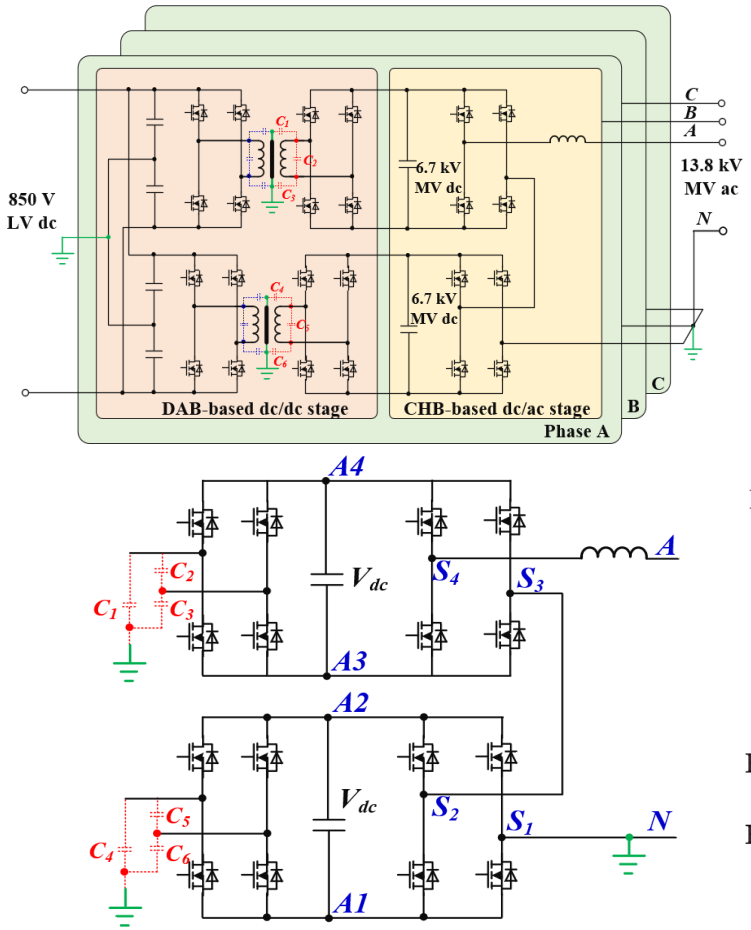


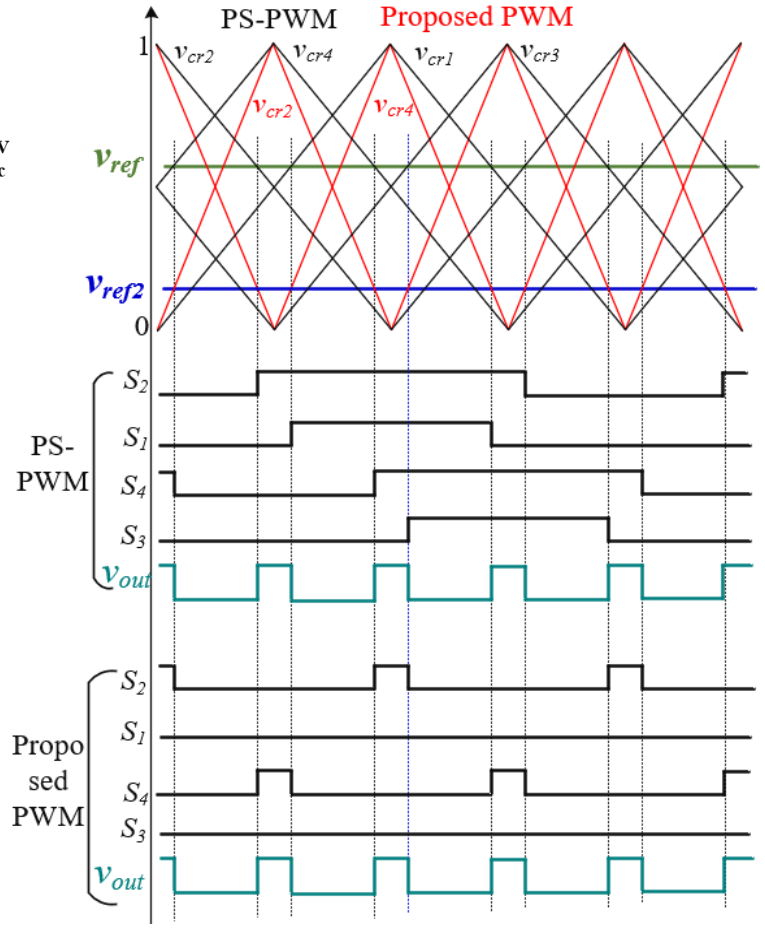
Low loss leakage integration structure & test results

[1] Z. Gao et al "A Medium-Voltage Transformer with Integrated Leakage Inductance for 10 kV SiC-Based Dual-Active-Bridge Converter", IEEE WIPDA 2022

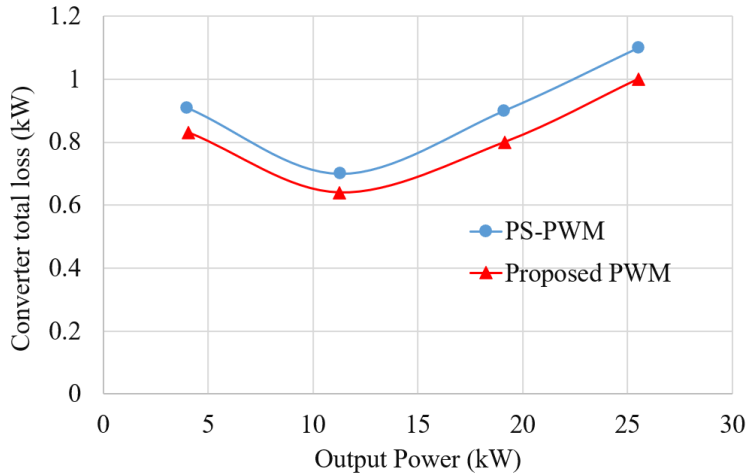
Transformer Parasitic Capacitance Caused Switching Loss

- Parasitic capacitance due to transformer grounding & shielding $P_{loss} \approx C_{para} V_{dc}^{\ 2} f_s$
- Modulation strategy developed to reduce the capacitive switching losses





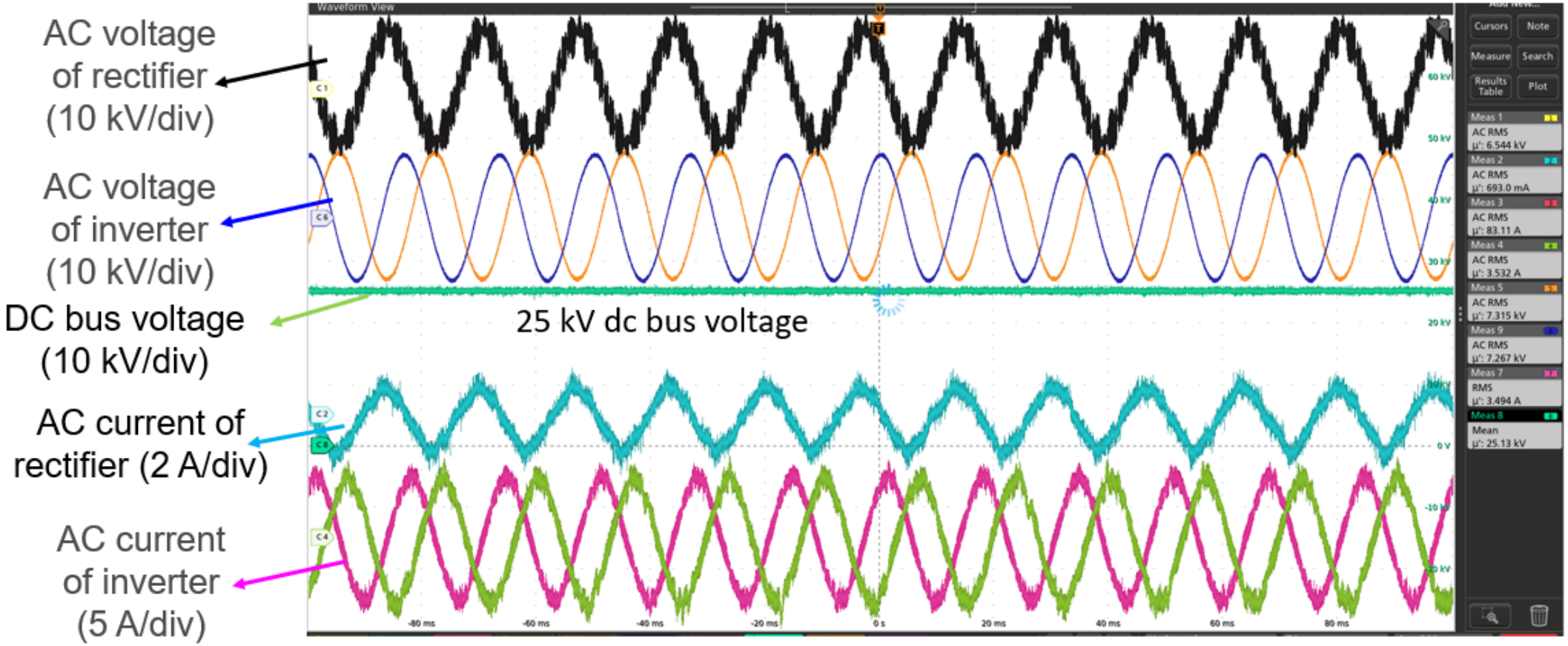
Parasitic capacitance	Equivalent voltage frequency		Parasitic Loss	
	PS-PWM	Proposed PWM	PS-PWM	Proposed PWM
C_1	9 kHz	3.12 kHz	43.6 W	15.1 W
C_3	9 kHz	3.12 kHz	43.6 W	15.1 W
C_4	3 kHz	60 Hz	14.5 W	0.3 W
C_6	3 kHz	60 Hz	14.5 W	0.3 W
Total			116 W	30.8 W



[1] H. Li et. al. "A PWM Strategy for Cascaded H-bridges to Reduce the Loss Caused by Parasitic Capacitances of Medium Voltage Dual Active Bridge Transformers" IEEE ECCE 2022

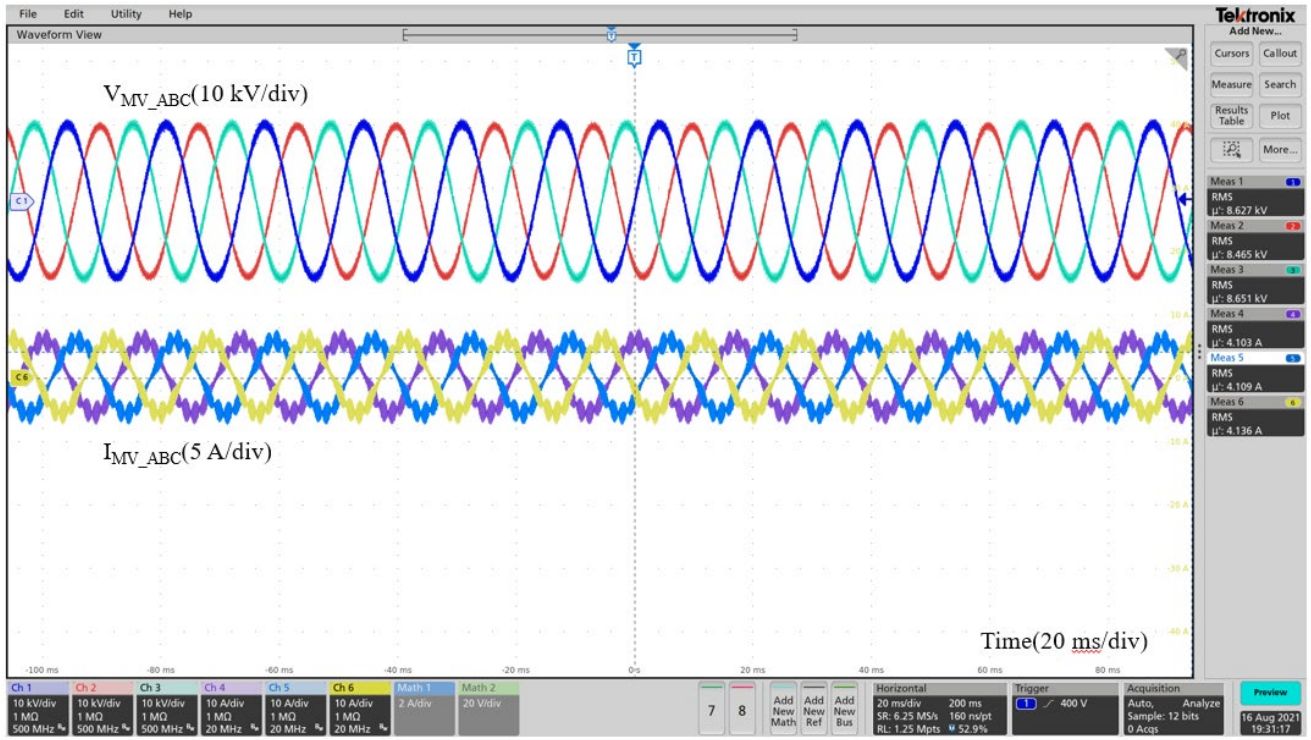
13.8 kV/ 100 kW PCS for Asynchronous Microgrid

- Full power test of the PCS module
  - Operation of back-to-back PCS module successfully achieved at 25 kV DC bus voltage
  - Control implemented to suppress 180 Hz common mode current



13.8 kV/ 100 kW Cascaded DC/DC and DC/AC PCS

- Line-to-line voltage: 14.9 kV RMS
- Power: 106 kVA



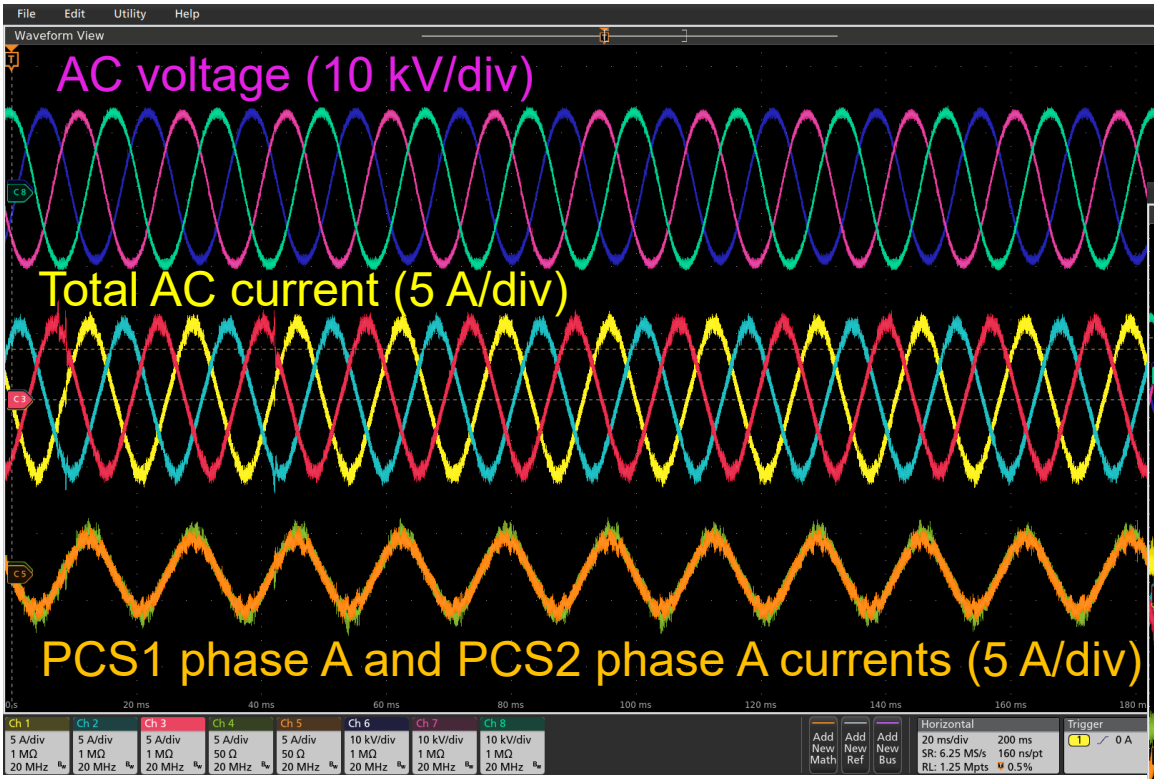
MV AC-side voltage and current waveforms

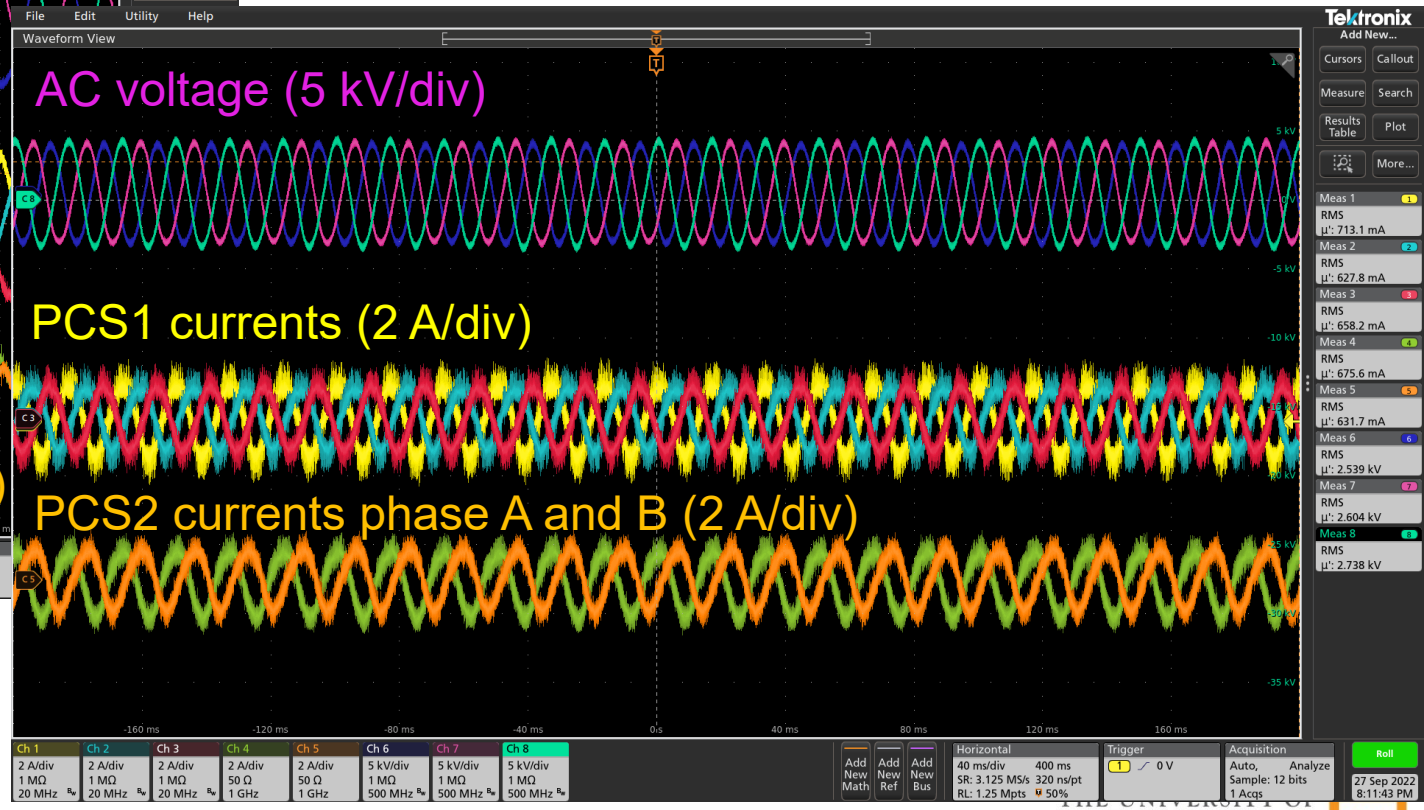
- Performances and functions tested

#	Category	Function
1	Converter performance	Full voltage and power rating operation (13.8 kV/100 kW)
2		Voltage THD ~ 2.72%
3		Current TDD ~ 0.8%
4		Efficiency ~ 96.4%
5		Voltage control bandwidth ~ 300 Hz
6		Current control bandwidth ~ 1.1 kHz
7	Grid requirements/functions	Var support (voltage support)
8		Frequency ride Through
9		Voltage ride through
11		Protection (over voltage, under voltage, over frequency, under frequency, etc.)
12		Balanced/unbalanced load support in the islanded mode

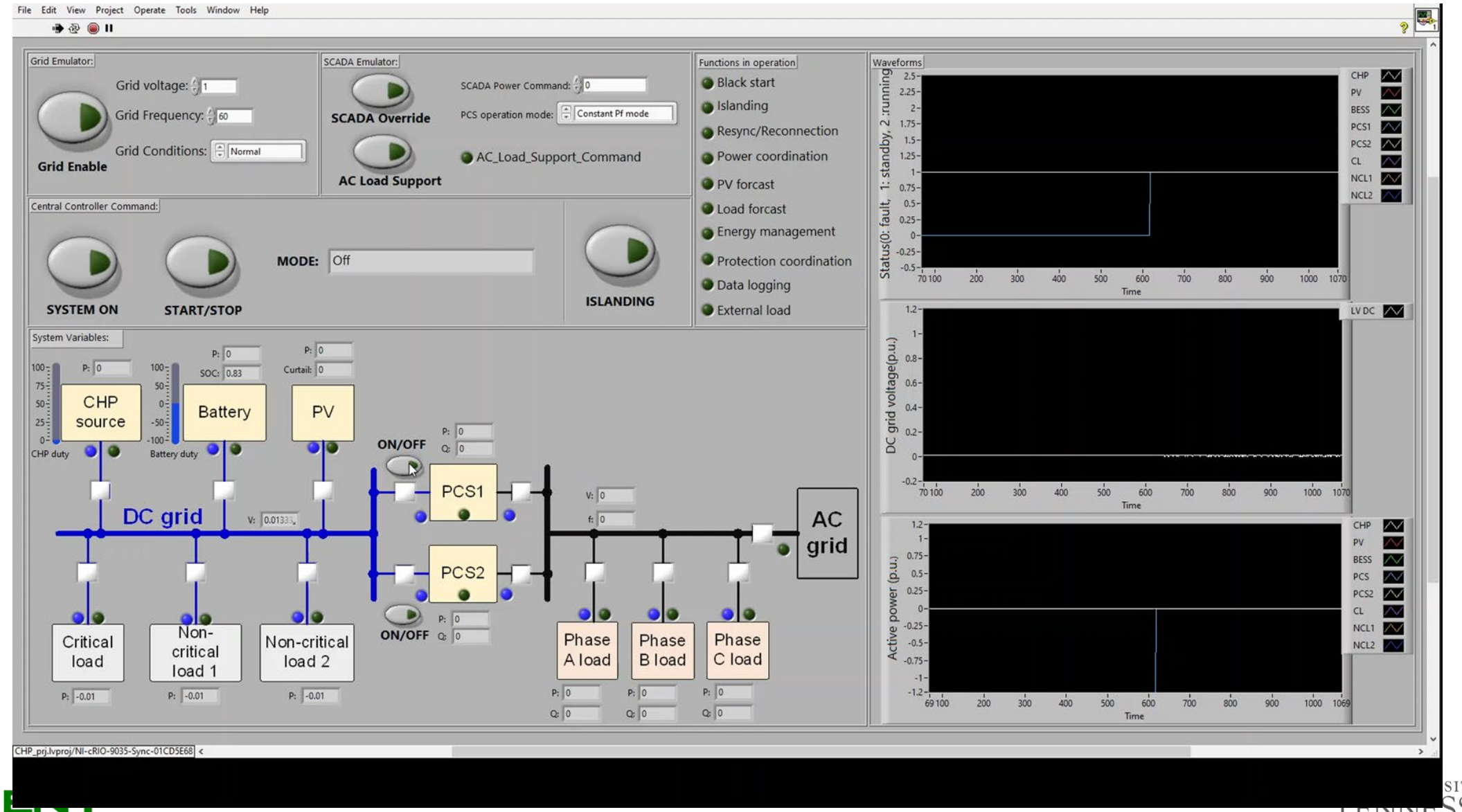
Scalable PCS Converter Testing

- Two PCS in parallel tested (13.8 kV RMS line-to-line) for grid-connected and islanded modes





PCS Controller Test on HTB



Summary

- MV SiC can benefit grid power electronics at both converter and system levels
- Grid requirements can significantly impact on MV power converter design
- Fast switching of MV SiC devices results in high *dv/*dt, which, together with high voltage, poses great challenges for converter design (noise immunity, insulation, parasitic loss)

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