Rapid Assessment of Power Module Reliability using Transient Thermal Analysis

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● Introduction to reliability
● Rapid assessment of degradation
● Transient thermal analysis
● Correlation with non-destructive characterisation
● Conclusions
● Region I infant mortality:
  ● Failure due to manufacturing faults etc.
  ● No meaningful lifetime prediction

● Region II constant failure rate:
  ● Mean Time Between Failure (MTBF) = total service time/number of failures
  ● No meaningful lifetime prediction

● Region III progressive wear-out
  ● Depends on in-service use
  ● Mean Time To Failure (MTTF)

● Lifetime prediction possible
Physics-of-Failure (PoF)

- Combined modelling and accelerated life testing
- Identify root cause (physics) of life-limiting degradation and failure mechanisms
- Develop predictive models for key degradation mechanisms
- Apply validated models to
  - Assess design options
  - Design improved accelerated tests
  - Prognostics and health management
Experimental Approach

1. Accelerated life tests through passive & power cycling, vibration, humidity etc.
2. Parallel studies of diffusion phenomena
3. Fine-scale microstructural characterisation
4. Formulation of empirical relationships & validation

Observations

- Failure mechanisms and models need to be valid for both accelerated test and in-service conditions
- Acceleration of desired mechanism may be masked by other failure mechanisms
- Destructive characterisation (e.g. shear test/cross-sectioning) prevents same sample analysis and cannot be done in real time
- Many samples required to build accurate picture of spread and uncertainty
# Key Wear-Out Mechanisms

<table>
<thead>
<tr>
<th>Interconnect type</th>
<th>Wear-out mechanism</th>
<th>Damage processes</th>
<th>Indicators</th>
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</thead>
<tbody>
<tr>
<td>SnAg/SAC solder</td>
<td>Cracking &amp; delamination</td>
<td>Creep &amp; TMF IMC growth/thickening alter bulk mechanical properties; Large IMCs help cracks to propagate; Creep voids speed up TMF</td>
<td>Increased Rth Crack propagation observed by SAM, X-ray CT Reduced shear strength Microstructural changes</td>
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<tr>
<td>Wire bonds Al-Al</td>
<td>Wire-bond lift-off, loop cracks</td>
<td>Thermomechanical stresses due to CTE mismatch leading to cracking at interface, heel and loop, residual surface oxide, IMC growth, creep, electromigration</td>
<td>Increased Vf Crack propagation observed by SAM, X-ray CT Reduced shear strength Microstructural changes</td>
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Rapid Assessment Methodology

- Power cycling e.g. using Mentor Graphics Power Tester 1500A
  - Constant current and constant (peak) temperature control strategies
  - In-situ voltage and temperature measurement
  - In-situ transient thermal analysis
- Non-destructive characterisation
  - Periodic assessment using X-ray computed tomography or Scanning Acoustic Microscopy
  - Provides validation of and correlation with $R_{th}$, Von measurement
- Post-test microstructural evaluation
- Thermal resistance of interface between module and tester cold-plate modified to alter relative temperature swing in different layers
  - Higher interface thermal resistance emphasises swing close to base-plate
  - Lower interface thermal resistance emphasises swing close to die
- Control strategy alters behaviour under degradation
  - Junction temperature control leads to reduced heating power as degradation progresses (increased $R_{\text{th}}$, $V_{\text{on}}$)
  - Current control leads to increased temperature swing (increased $R_{\text{th}}$) and/or heating power (increased $V_{\text{on}}$)
- Module mounted on water-cooled heatsink with a 25 μm Kapton film to achieve ΔT≈70°C at the substrate (measured by integrated NTC)
- Current and junction temperature control strategies
- Transient thermal impedance measured every 1000 cycles
- Power cycling test was interrupted regularly and modules were removed for Scanning Acoustic Microscopy (SAM)
Comparison of Control Methods

- **Constant current**
  - **Max Tj**
  - **Vce**

- **Constant ΔT**
  - **Max Tj**
  - **Vce**

**Failure mode**
- Solder fatigue
- Wire bond lift-off + solder fatigue
● After 12500 cycles, wire bond foot imprints in the two IGBTs on the middle substrate became less distinct indicating the start of wire bond lift-off

● After 21,000 cycles significant degradation of the solder layer between substrate and base-plate
● Increased delaminated area with increased number of power cycles
● Delamination initiates at edge of substrate and propagates towards the centre

Attached area calculated by MATLAB software
Cumulative structure function

- Plot of cumulative thermal capacitance vs. cumulative thermal resistance

0-6,000 cycles: no obvious changes observed below $R_{th}=0.06$ (K/W) indicating no significant extent of degradation in the heat flow path from chip to the baseplate
Cumulative Structure Function

7000-17000 cycles

- Signs of degradation in the heat flow path with a maximum $R_{th}$ variation of 47.8%

- Changes indicative of increasing thermal resistance: curves shifted to the right as the test proceeded
Thermal Resistance

- Junction-to-case thermal resistance $R_{thjc}$ can be measured from the structure function between the case layer and the Kapton film layer.
- Correlated with attached area from SAM images.
- Increase in $R_{thjc}$ is presumed to be related to solder fatigue.
- Plot of $K$ vs. cumulative $R_{th}$: $K_\Sigma = \frac{dC_\Sigma}{dR_\Sigma} = \lambda cA^2$
- Each peak represents a specific material in the thermal stack
- Value of $K$ is proportional to the squared cross-sectional area
- No sign of degradation in module thermal path before 6000 cycles
From 7000-15000 cycles amplitudes of some peaks decline and shift.

The decreased amplitude in Peak 2 and Peak 3 indicates a reduced effective thermal cross-sectional area within the substrate solder and base-plate.

Horizontal shift of Peak 3 reveals an increase in the thermal impedance of the solder layer.
The $K$-value determined from transient thermal impedance measurements agrees well with the attached area, as determined by scanning acoustic microscopy.

Differential structure function and $K$-value can be used to quantify the level of degradation in different layers of the thermal path.
Confirmation of Degradation Mechanism

- Metallurgical cross-sectioning confirmed that cracking took place at the substrate-base-plate interface
- Cracks occurred in the substrate-to-baseplate solder layer from the edge, emanating at the interface between the solder and the bottom Cu DBC layer
- DBC itself survived without any delamination
- No obvious voids or edge cracks were observed in the die attach layer

Cross-sectional optical microscopy
Conclusions

● Reliability studies essential to many power electronic components and systems

● Detailed understanding of wear-out mechanisms needed to:
  • Develop models for design and prognosis
  • Understand impact of manufacturing processes & materials
  • Quantify variability

● Rapid assessment of degradation under thermal cycling enabled by power cycling coupled with on-line measurement of key degradation indicators

● Selection of dominant degradation mechanism:
  • Modification of base-plate to cold-plate thermal resistance
  • Change of control strategy

● Transient thermal impedance analysis provides a means for rapid quantitative assessment of thermal path degradation
  • Correlated with detailed characterisation using non-destructive techniques e.g. SAM X-ray CT