Design Optimisation and Trade-offs in Multi-kW DC-DC Converters

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Abstract—This work investigates design optimisation and design trade-offs for multi-kW DC-DC Interleaved Boost Converters (IBC). A general optimisation procedure for weight minimisation is presented, and the trade-offs between the key design variables (e.g. switching frequency, topology) and performance metrics (e.g. power density, efficiency) are explored. It is shown that the optimal selection of components, switching frequency, and topology are heavily dependent on operating specifications such as voltage ratio, output voltage, and output power. With the device and component technologies considered, the single-phase boost converter is shown to be superior to the interleaved topologies in terms of power density for lower power, lower voltage specifications, whilst for higher-power specifications, interleaved designs are preferable. Comparison between an optimised design and an existing prototype for a 220 V - 600 V, 40 kW specification, further illustrates the potential weight reduction that is afforded through design optimisation, with the optimised design predicting a reduction in component weight of around 33%.

I. INTRODUCTION

Modern power electronics designs are subject to ambitious performance targets, such as high power density, efficiency and reliability. This is driven by application areas such as automotive [1] and renewable energy [2]. A number of enabling technologies exist for such converters, including liquid-cooling, interleaved and soft switching topologies, new magnetic materials, improved component structures, and emerging semiconductor devices, such as SiC diodes and MOSFETs. To capitalise fully on these enabling technologies, multi-domain modelling and design optimisation techniques are needed, allowing improved designs in terms of power density, efficiency, or reliability. Optimisation techniques also provide a convenient platform for exploring the key trade-offs, e.g. the variation of minimum weight or maximum efficiency with switching frequency or device selection. Previous works have proposed design optimisation techniques for numerous topologies and applications, e.g. [3]–[7].

This work investigates the design optimisation of multi-kW DC-DC converters, and identifies the key design trade-offs. These converters form building blocks in a number of emerging applications, such as automotive power trains, photovoltaic power generation, and more-electric aircraft. In particular, the Interleaved Boost Converter (IBC) with an Interphase Transformer (IPT) is considered. Compared to discrete inductors, the IPT has been stated to offer potential reductions in weight and volume [8]–[10], and increased reliability [11]. In [8], an IPT is compared against discrete inductors for a particular 8 kW design, with the conclusion being that the IPT offers a significant saving in weight and volume. In [9], it is found that, for a particular 1 kW specification, the IPT-based solution can offer sizable reductions in volume relative to a design with discrete inductors. In [10], a four-phase IBC is considered for a 56 kW specification, with the results again showing that a transformer-based solution offers a significant improvement in power density relative to discrete inductors.

Although the aforementioned works have investigated various IBC designs, the holistic design optimisation of the IPT-based IBC is a topic that has received little specific attention. We therefore address this by presenting a design optimisation procedure. The proposed strategy, which aims to minimise the weight of the converter, is also applicable to the IBC with discrete inductors, enabling comparison between the two. Due to the large number of design variables that are involved and which can influence the weight of the converter - e.g. the device selection, switching frequency, and magnetic parameters - this is an interesting and important area of study. Related works include [3], which deals with the optimisation of a multi-phase DC-DC converter. However, [3] restricts the free design variables to the phase count and the switching frequency, and unlike this work does not consider magnetic coupling between the converter phases.

In order to validate the proposed optimisation strategy, we compare the results against the IBC described previously in [12] as an example of a design which is power-dense (11.5 kW/kg and 20.0 kW/l), but not necessarily optimal. Comparing optimised designs with this example provides a way to evaluate the efficacy of both ‘standard’ design techniques and those that are based on holistic design optimisation. In order to further verify the results, experimental measurements are used to validate the device and component models that are used.

In terms of overall contribution, this paper provides insights into the design trade-offs in multi-kW DC-DC converters, and provides a rigorous basis for the selection of IBC topology and components.

II. INTERLEAVED BOOST CONVERTER

Fig. 1(a) shows a schematic of a two-phase IBC with discrete inductors, whilst Fig. 1(b) shows a two-phase IPT-based IBC. Among the benefits of the IBC are ripple cancellation at the input and output and increased ripple frequency, potentially enabling reductions in the size of the passive components. At particular power levels and switching frequencies, and with certain components, the IPT-based topology has been shown
to offer further reductions in size compared to the discrete topology [13], [14]. However, it remains unclear as to whether this is true in general.

A. Prototype IBC

Fig. 2 pictures a prototype IBC, which was designed with an input voltage of 220 - 380 V, an output voltage of 600 V, and an output power of between 40 and 60 kW. It has power densities of 11.5 kW/kg and 20.0 kW/l at full load, and provides an example of the type of assembly that is considered in this work. The inductor and IPT cores are nanocrystalline metal and are wound with copper foil. Film capacitors are used in this work. The inductor and IPT cores are nanocrystalline and (b) coupled phases.

III. OPTIMISATION PROCEDURE

The task of power converter design is approached as a discrete optimisation problem. Inputs to the algorithm include the design specifications (i.e. the input and output voltages and output power), constraints (e.g. maximum output voltage ripple or inductor current ripple) and a design objective, which for this study is restricted to minimisation of weight. The algorithm assesses each possible solution within the design space, with the design that offers the lowest weight, while also satisfying the constraints, being deemed the optimal design. This method is fairly general and can be applied to a range of power electronics design problems, with the combinatorial framework being a good fit for the discrete nature of electronic components. Each of the \( n \) design variables \( x_1 \) - \( x_n \) is limited taking values belonging to a finite set, \( \mathcal{X}_1 - \mathcal{X}_n \), each of size \( N_1 - N_n \), i.e.

\[
x_1 \in \mathcal{X}_1, \quad \mathcal{X}_1 = \{x_1^{(1)}, x_1^{(2)}, ..., x_1^{N_1}\}
\]

\[
\vdots
\]

\[
x_n \in \mathcal{X}_n, \quad \mathcal{X}_n = \{x_n^{(1)}, x_n^{(2)}, ..., x_n^{N_n}\}.
\]

Each overall design is denoted \( x = [x_1 x_2 ... x_n] \), and the total number of possible designs is given by \( |\mathcal{X}| = N_1 N_2 ... N_n \).

Further details of the chosen optimisation framework can be found in [15].

A. Application to the IBC

The design variables for the optimisation of the IBC are summarised in Table I. For the IPT-based IBC, the phase count is fixed at two, and for the single-phase boost converter/IBC with discrete inductors, the variables relating to the IPT are redundant.

As stated, the design objective is to minimise the weight, \( w \), of the converter. The constrained values include the efficiency, \( \eta \), the junction temperature, \( T_j \), the inductor winding (\( T_w \)) and core (\( T_c \)) temperatures, the input capacitor voltage ripple, \( \Delta V_{in} \), the output capacitor voltage ripple, \( \Delta V_{out} \), and the peak flux density in the inductor core, \( B_{l,pk} \). Additionally, the input and output capacitors need to be rated to handle the RMS current, \( I_{C_i,rms} \) and \( I_{C_o,rms} \). The optimisation problem can now be stated in full as

\[
\text{Minimise: } w(x)
\]

Subject to: \( x \in \mathcal{X} \)

\[
-\eta(x) \leq -\eta_{\text{min}}
\]

\[
T_j(x) \leq T_{j,\text{max}}
\]

\[
T_w(x) \leq T_{w,\text{max}}
\]

\[
T_c(x) \leq T_{c,\text{max}}
\]

\[
\Delta V_{in}(x) \leq \Delta V_{in,\text{max}}
\]

\[
\Delta V_{out}(x) \leq \Delta V_{out,\text{max}}
\]

\[
B_{l,pk}(x) \leq B_{l,\text{max}}
\]

\[
I_{C_i,rms}(x) \leq I_{C_i,\text{rms,max}}(x)
\]

\[
I_{C_o,rms}(x) \leq I_{C_o,\text{rms,max}}(x)
\]

TABLE I: Design variables for the optimisation of the IBC.

<table>
<thead>
<tr>
<th>Design variable</th>
<th>Symbol</th>
<th>Design variable</th>
<th>Symbol</th>
</tr>
</thead>
</table>
| Switching frequency | \( f \) | IPT core | \( U_{1\text{IPT}} \)
| No. phases | \( N_p \) | Turns per IPT | \( N_{1\text{IPT}} \)
| No. modules per phase | \( N_M \) | Input capacitor model | \( C_i \)
| Module type | \( M \) | No. input capacitors | \( N_i \)
| Inductor core | \( U_L \) | Output capacitor model | \( C_o \)
| Turns per inductor | \( N_L \) | No. output capacitors | \( N_o \) |
The final three constraints are not fixed, but vary according to each particular design $x \in X$. The capacitor current ripple constraints vary with the type and number of capacitors. For the IPT-based IBC, additional constraints are introduced - the IPT core ($T_{c,IPT}$) and winding ($T_{w,IPT}$) temperatures, the IPT current ripple, $\Delta I_{IPT}$, and the peak IPT flux density, $B_{IPT, pk}$, i.e.

$$T_{c,IPT}(x) \leq T_{c,IPT,\text{max}}$$
$$T_{w,IPT}(x) \leq T_{w,IPT,\text{max}}$$
$$B_{IPT, pk}(x) \leq B_{IPT,\text{max}}$$ (3)

An additional constraint is for the converter to operate in continuous conduction mode.

IV. COMPONENT MODELS

For each design, a set of models which describe the electrical and thermal behaviour of the converter are used to calculate the values of the constrained quantities, which are checked against their respective constraints. For those designs that are feasible, i.e. which satisfy each of the constraints, a separate set of models is used to calculate the weight of the design. The models that are presented assume an IPT-based IBC, but are easily adapted for the single-phase boost converter and IBC with discrete inductors. The models are based on the components used in the prototype pictured in Fig. 1, and can be outlined as follows:

- **Semiconductors:** The semiconductor models are based on half-bridge SiC MOSFET (CREE/Wolfspeed CAS100H12AM1 and CAS300M12BM2) modules [16], rated to 1200 V, and 100 and 300 A, respectively. The modules are mounted directly to the surface of the cold plate.

- **Inductors:** The inductor and IPT cores are selected from the FINEMET F3CC range of nanocrystalline metal cores [19]. The cores are C-shaped, with a maximum temperature of 155°C, and saturation flux density of 1.2 T. Copper foil is considered for the inductor and IPT windings. The inductors are assumed to be potted in aluminium cans with an epoxy filling, with the bases of the cans directly mounted to the surface of the cold plate. Fig. 3 illustrates the construction of the magnetic components.

- **Cold plate:** The cold plate is liquid cooled and is sized for each design based on the area that is required to mount the modules and inductor/IPT, and is not treated as an independent design variable.

A. Models for Constraints

A converter model is required to evaluate whether or not a design satisfies the constraints listed in (2) and (3). The first step is to calculate the duty cycle, $D$, assuming continuous conduction

$$D = \frac{V_{out} - V_{in}}{V_{out}}.$$ (4)

The inductance of the input inductor is a function of the inductor U-core, $U_L$, and the number of turns, $N_L$, i.e.

$$L = \frac{4\pi N_L^2 A_c F_c}{l_g} \times 10^{-7}$$ (5)

where $A_c$ is the core area for the core index $U_L$, $F_c$ is the fringing factor, and $l_g$ is the total length of the air-gap of the core. The self inductance of each winding of the IPT is similarly given in terms of the IPT U-core, $U_{IPT}$, and the number of turns for the IPT, $N_{IPT}$, by

$$L_{IPT} = \frac{\pi N_{IPT}^2 A_{c,IPT} F_{c,IPT}}{l_{g,IPT}} \times 10^{-7}$$ (6)

and the mutual inductance by

$$L_m = k L_{IPT}$$ (7)

where $A_{c,IPT}$, $F_{c,IPT}$, and $l_{g,IPT}$ have the same meanings as for the inductor, and where $k$ is the coupling factor, assumed to be 0.98. The input and output capacitance, $C_{in}$ and $C_{out}$, are given by

$$C_{in} = C(C_i)N_i, \quad C_{out} = C(C_o)N_o$$ (8)

where $C(C_i)$ and $C(C_o)$ return the capacitances corresponding to the indices, $C_i$ and $C_o$, respectively. With $L$, $L_{IPT}$, $L_m$, $C_{in}$, and $C_{out}$ calculated, along with the switching frequency $f$, the constrained values $\Delta V_{in}(x)$, $\Delta V_{out}(x)$, $\Delta I_l(x)$, $I_{C,rms}(x)$, $I_{C_o,rms}(x)$, and $\Delta I_{IPT}(x)$ can then be calculated along with the average values of the inductor and IPT currents, $I_l$ and $I_{IPT}$, as $I_l$ and $I_{IPT} \equiv I_l/2$.

The conduction, turn-on, and turn-off losses in the diode and MOSFET in each module can be calculated using equations which are fitted according to datasheet loss specifications. The coefficients in the loss equations vary with each module $M$ in the design space. The total loss in the modules is denoted $P_M = P_{m} + P_{d}$, where $P_{m}$ is the total loss in the MOSFET, and $P_{d}$ the total loss in the diode.

The inductor losses are separated into two components - the core losses, $P_c$, and the winding losses, $P_w$. The core loss has two components - the hysteresis component, $P_h$, and the gap-loss component, $P_g$, i.e. $P_c = P_h + P_g$. The first term, for the hysteresis component, is calculated using the peak-to-peak flux density in the core, $\Delta B_l$, the weight of the inductor core,


The winding losses, $P_w$, and the switching frequency of the design. The value of $\Delta B_1$ is found from

$$\Delta B_1 = 4\pi N I_a F_c \Delta h \times 10^{-7}. \quad (9)$$

From the manufacturer-provided loss curves, a Steinmetz-type equation emerges, being written as

$$P_h = k_w w f^\alpha \left( \frac{\Delta B_1}{2} \right)^\beta \quad (10)$$

where the coefficients for the FINEMET nanocrystalline cores are taken as $k_w = 1.25 \times 10^{-5}$, $\alpha = 1.69$, and $\beta = 2$. Because the core losses arise due to hysteresis effects, they are assumed to be distributed evenly throughout the core. The second term, for the gap loss, can be expressed as

$$\Delta \ = 1.68 \beta f^\gamma = \frac{10^3}{2} \times 10^{-3} \quad (11)$$

where $1.68 \times 10^{-3}$ is a fixed constant and $h_c$ is the lamination width. The equation in (11) is empirical and taken from the finite element simulations and experimental measurements detailed in [20]. The gap losses are centered around the faces of the core gaps.

The winding losses, $P_w$, are computed via Dowell’s method [21], using the first ten harmonics of the inductor currents. With this method, the DC resistance of the winding is mapped to an ‘effective’ AC resistance, $R_{l,ac}$, with the losses in the winding then given by

$$P_w = I_{rms}^2 R_{l,ac} \quad (12)$$

where $I_{rms}$ is the RMS inductor current. The total losses in the inductor are then given by $P_I = P_c + P_w$.

The losses in the IPT can be calculated in a similar way to those of the inductor. The hysteresis component of the IPT losses, $P_h_{IPT}$, is calculated in the same way as the inductor, where the peak-to-peak flux density in the core, $\Delta B_{IPT}$, the weight of the core, $w_{IPT}$, and the switching frequency of the design are substituted into (10). The value of $\Delta B_{IPT}$ is given by

$$\Delta B_{IPT} = \begin{cases} \frac{V_{out}}{f N_{IPT} A_{IPT}} & \text{if } D \leq 0.5 \\ \frac{V_{out}(1-D)}{f N_{IPT} A_{IPT}} & \text{if } D > 0.5 \end{cases} \quad (13)$$

The IPT gap loss, $P_g_{IPT}$, can be found using (11), where $I_{IPT}$, $h_{IPT}$, and $\Delta B_{IPT}$ are substituted in as appropriate. The winding losses, $P_w_{IPT}$, are computed in the same way as for the inductor, using the AC resistance of each winding, $R_{IPT,ac}$, and the RMS current through each branch of the IPT, $I_{IPT,rms}$. The total losses in the IPT are then given by $P_{IPT} = P_h_{IPT} + P_w_{IPT}$. The converter efficiency, $\eta$, can then be computed using $^1$

$$\eta = 100 \frac{P_{out} - (2N M P_M + P_l + P_{IPT})}{P_{out}} \quad (14)$$

The thermal calculations are based on lumped-parameter heat flow models, under the assumption that the dominant heat flow mechanism is conduction, with the heat flowing towards the surface of the cold plate. The junction temperature within each module, $T_j$, is defined as the greater of the MOSFET, $T_m$, and diode, $T_d$, temperatures, and can be written as

$$T_j = \max(P_m R_{th,m} + P_d R_{th,d}) + (P_m + P_d) R_{th,p} + T_a \quad (15)$$

where $R_{th,m}$ is the thermal resistance between the MOSFET and the case of the module, $R_{th,d}$ is the thermal resistance between the diode and the case of the module, $R_{th,p}$ is the thermal resistance of the thermal paste between the module and cold plate, and $T_a$ is the inlet/ambient temperature, assumed to be approximately equal to the temperature of the cold plate surface.

The heat generated in the winding is modelled as being concentrated at specific points within the copper windings, and is assumed to flow through the winding material to the aluminium case of the inductor. The heat generated in the core is modelled as flowing from the centre of the core and through the lower part of the winding to the aluminium case. The thermal resistances are calculated based on the geometries and material properties of each inductor/IPT design. Due to space constraints, a detailed description of the model is not included.

**B. Models for Objective Function**

For a given design $x$, the weight is given by

$$w(x) = w_C + w_L + w_{IPT} + w_M + w_{CP} \quad (16)$$

where $w_C$ is the weight of the capacitors, $w_L$ is the weight of the inductor, $w_{IPT}$ is the weight of the IPT, $w_M$ is the weight of the modules, and $w_{CP}$ is the weight of the cold plate. The key information relating to each component in the design space is contained in a database of look-up tables. Denoting the weight of the input and output capacitors within a design as $w(C_1)$ and $w(C_o)$, respectively, the total capacitor weight is given by multiplying both by the respective number that are connected in parallel, i.e.

$$w_C = N_i w(C_1) + N_o w(C_o) \quad (17)$$

Similarly, each inductor core occupies a row in a look-up table with the same basic structure as the capacitor table, and the weight of each inductor core can be taken from the table. The weight of the winding is calculated from the core dimensions, number of turns, and copper foil properties. The weights of the aluminium can and the potting compound, which are determined from the dimensions of the core and winding, are then calculated. The total weight of the inductor is given by

$$w_{IPT} = w_U + w_N + w_A + w_E \quad (18)$$

where $w_U$ is the weight of the core, $w_N$ the weight of the winding, and $w_A$ and $w_E$ are the weights of the aluminium can and epoxy, respectively. The weight of the IPT, $w_{IPT}$, can be determined in the same fashion as for the inductor.

The weight of the individual modules used in each design is denoted $w_{Mod}$, and the total module weight is given by

$$w_M = 2N_M w_{Mod} \quad (19)$$

^1Note that, due to the very low impact they have on the efficiency of the system, capacitor losses are not considered when calculating efficiency.
The cold plate is sized to accommodate the modules and magnetic components. Several layouts are considered, and the one which requires the smallest cold plate surface area is deemed best for the design. The weight of the cold plate is then determined using a set of parameters corresponding to a pin-fin liquid cooled concept.

V. RESULTS

A. Model Validation

In order to validate the models, they are compared against experimental measurements from the prototype IPT-based IBC pictured in Fig. 2. The inlet temperature of the cold plate is \( T_a = 40^\circ C \). Validation is performed by fixing the design variables in the optimization algorithm to those used in the prototype converter, and comparing the losses, efficiency and estimated weight of the components.

The inductor core is the FINEMET F3CC0032, with six turns of 0.8mm thick copper foil winding and an air gap of 4.4mm. Table II compares the total inductor losses predicted by the model against experimental measurements obtained at three different operating points - 50-200 V, 70-280 V, and 120-300 V, each with an average input current of 160 A and a switching frequency of 30 kHz. It can be seen that the two sets of results show good agreement.

In order to validate the device models, the predicted losses of the CAS100H12A12 module are compared against the experimental measurements. Table III compares the switching and conduction losses, with \( V_{\text{in}} = 380 \text{ V}, V_{\text{out}} = 600 \text{ V}, P_{\text{out}} = 60 \text{ kW}, \text{ with } f_{\text{sw}} = 75 \text{ kHz}. \) It can be seen that close agreement is again shown between the predicted and measured values, with the relative error between the two being about 3%.

The overall efficiency of the converter was measured at 97.5% for 220 - 600 V, 40 kW operation, and 98.7% for 380 - 600 V, 60 kW operation. The predicted efficiencies based on the models are 97.7% and 98.6%, respectively, meaning that the nominal loss predictions for the complete converter are accurate to within a few percent for both operating conditions.

The predicted weight of the inductor and IPT are compared against the measured values in Table IV. It can be seen that the model provides a good estimate of the individual weights of the inductor and IPT, as well as the combined assembled weight (which includes the cans and epoxy), the latter being within 1.5% of the measured value.

B. Optimisation Results

The results of the design optimisation procedure, and the design trade-offs that emerge from this process, are now examined for several different case studies. The design space that was considered is summarised in Table V. The assumed inlet temperature for the cold plate is 60°C. The efficiency was restricted to being above 95%, the junction and winding temperatures were restricted to 150°C, and the core temperature was restricted to 155°C. The input and output voltage ripples were restricted to 5% and 2%, respectively. The peak flux density in the inductor and IPT cores is limited to 1.1 T.

Fig. 4 shows the variation of the minimum weight, and corresponding efficiency, for the full range of switching frequencies that were considered. The output voltage and power are fixed at 600 V and 60 kW, respectively. Three different input voltages are considered - 220 V, for which the duty cycle is 0.63 and for which the input current is relatively high, 300 V, for which the duty cycle is 0.5 and the input current is moderate, and 450 V, for which the duty cycle is 0.25 and the input current is relatively low.

Fig. 4(a) shows the weight trend with \( V_{\text{in}} = 220 \text{ V}. \) As the frequency increases from 20 to 90 kHz, the minimum weight reduces from just under 6 kg to 3.56 kg. This is driven mainly by a reduction in the weight of the inductor and IPT. If the inductance values of the inductor/IPT are held constant as the frequency increases, the flux ripples tend to decrease. Consequently, as the frequency increases the inductance values can instead be reduced without increasing the ripple/losses, enabling smaller cores with fewer turns to be used for both the inductor and IPT. Above 90 kHz, it can be seen that no further reductions in weight can be achieved, due to the thermal limits of the inductor cores. A sharp increase in weight is then observed at 120 kHz, where a jump from the 100 A modules to the heavier 300 A modules occurs due to the increasing switching losses. The efficiency for the optimal design (at 90 kHz) is just under 98%, as seen in Fig. 4(d).

Fig. 4(b) shows the same trend with \( V_{\text{in}} = 300 \text{ V}. \) The

<table>
<thead>
<tr>
<th>Design variable</th>
<th>Range of values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Losses</td>
<td>50-200 V</td>
</tr>
<tr>
<td>Model (W)</td>
<td>123</td>
</tr>
<tr>
<td>Meas. (W)</td>
<td>110</td>
</tr>
</tbody>
</table>

TABLE II: Comparison of total inductor losses - model and experimental measurements. The average input current is 160 A, the peak-to-peak inductor current ripple is 130 A, and the device switching frequency is 30 kHz.

<table>
<thead>
<tr>
<th>Losses</th>
<th>Switching</th>
<th>Conduction</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model (W)</td>
<td>159</td>
<td>35</td>
<td>194</td>
</tr>
<tr>
<td>Meas. (W)</td>
<td>162</td>
<td>38</td>
<td>200</td>
</tr>
</tbody>
</table>

TABLE III: Comparison of MOSFET losses in each phase - model and experimental measurements. The input voltage is 380 V, the output voltage is 600 V, the output power is 60 kW, and the switching frequency is 75 kHz.

<table>
<thead>
<tr>
<th>Weight</th>
<th>Inductor</th>
<th>IPT</th>
<th>Assembled total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model (kg)</td>
<td>0.71</td>
<td>0.98</td>
<td>2.61</td>
</tr>
<tr>
<td>Meas. (kg)</td>
<td>0.72</td>
<td>1.03</td>
<td>2.58</td>
</tr>
</tbody>
</table>

TABLE IV: Comparison of the estimated weight of the inductor and IPT - model and measured values.

<table>
<thead>
<tr>
<th>Design variable</th>
<th>Range of values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module</td>
<td>CAS100H12A12, CAS300M12BM2</td>
</tr>
<tr>
<td>No. phases (( \equiv 2 ) for IPT-IBC)</td>
<td>{1, 2}</td>
</tr>
<tr>
<td>No. modules per phase</td>
<td>{1, 2, 3}</td>
</tr>
<tr>
<td>Inductor core, IPT core</td>
<td>Finemet F3CC series (12 total)</td>
</tr>
<tr>
<td>Turns per inductor</td>
<td>{2, 4, ..., 24}</td>
</tr>
<tr>
<td>Turns per IPT</td>
<td>{4, 8, ..., 28}</td>
</tr>
<tr>
<td>Input capacitor model</td>
<td>TDK Ceramink, B3277 series (12 total)</td>
</tr>
<tr>
<td>No. input capacitors</td>
<td>{1, 2, ..., 10}</td>
</tr>
<tr>
<td>Output capacitor model</td>
<td>TDK B3277 series (11 total)</td>
</tr>
<tr>
<td>No. output capacitors</td>
<td>{1, 2, ..., 10}</td>
</tr>
</tbody>
</table>
minimum weight again occurs at 90 kHz, being 2.96 kg. Due to the perfect input ripple cancellation that occurs with \( D = 0.5 \), the input inductor has both the smallest core and fewest turns possible from the minimum frequency of 20 kHz onwards, whereas the IPT, which sees maximum ripple at fewest turns possible from the minimum frequency of 20 kHz and 1.36 kg at 90 kHz. Between 90 kHz and 180 kHz no further weight reduction is observed, and at 180 kHz a jump from 100 A to 300 A modules causes the weight to increase, and the efficiency to significantly decrease. The efficiency for the optimal design, as seen in Fig. 4(e) is 98.5\%, higher than the previous example due to the lower average currents in the inductor, IPT and switches.

Fig. 4(c) shows the trend with \( V_{in} = 450 \text{ V} \), for which \( D = 0.25 \). In this instance, the inductor is larger than the IPT, due to the high-level of ripple cancellation that is observed for the IPT at this duty cycle. Both magnetic components show some reduction in size as the frequency increases. The minimum weight of 2.78 kg is observed at 115 kHz, a slightly lower weight than for \( D = 0.5 \). Despite the higher input voltage causing a further reduction in the average currents, the efficiency of the optimal design, shown in Fig. 4(f), is 98.7\%, which is marginally higher than for the previous example.

Fig. 5 shows the envelopes of efficiency vs. power density among the three topologies at each of the duty cycles, \( D = 0.25, 0.5 \) and 0.75. It can be seen that for this output specification, the single-phase boost converter offers the highest feasible power density among the three topologies at each of the duty cycles, and for \( D = 0.25 \), the single-phase converter offers a nearly 40\% higher power density than the IPT-based IBC.

Fig. 6 shows the same trends with the output voltage increased to 600 V. The increased voltage across the inductors/IPT results in a reduction in the feasible power densities for each of the topologies, due to the heavier magnetic components that are required. Additionally, a much wider spread in the efficiencies of the feasible design envelopes is visible than in Fig. 5. Each of the topologies offer similar power densities, with the single-phase boost converter being slightly better at each duty cycle.

Fig. 7 shows the same trends as Fig. 6, with the output power increased to 60 kW, and with duty cycles of \( D = 0.25 \), 0.5 and 0.63, which limits the average input current to around 275 A. For this specification, it is clear that the single-phase topology is at a disadvantage to the multi-phase topologies; with \( D = 0.25 \), it offers a similar envelope to the others, but for \( D = 0.5 \) has a very small envelope, offering a much lower maximum power density than the IPT-based IBC, and, due to

\(^2\)For the results shown in Figs. 5 - 7, the efficiency constraint has been removed in order to fully evaluate the power density-efficiency trade-off.
the high input current, not offering any feasible solutions with \( D = 0.63 \). The two-phase IBCs have similar envelopes with \( D = 0.25 \), but for the higher duty cycles, the IPT-based solution clearly offers higher power densities.

Table VI provides a comparison between the prototype converter, pictured in Fig. 2, and an optimised IPT-based IBC design. Optimisation is performed at the lower voltage, lower power end of the prototype’s specification, i.e. \( V_{\text{in}} = 220 \text{ V} \), \( V_{\text{out}} = 600 \text{ V} \), and \( P_{\text{out}} = 40 \text{ kW} \). The prototype has a switching frequency of 75 kHz, whilst the optimised design has a slightly higher switching frequency of 80 kHz. It can be seen that weight reduction is achievable through the IPT, inductor, capacitors and cold plate, which combine for a 45% reduction in weight. Even discounting the weight of the cold plate, and focusing only on the components that are selected via independent design variables, a combined component weight reduction of 33% is predicted for the optimised design.

VI. CONCLUSIONS

A design optimisation strategy has been presented for multi-kW boost converters/IBCs, and the trade-offs between the key variables (switching frequency, topology) and performance metrics (power density, efficiency) have been explored. It
was shown that increased switching frequencies are beneficial in reducing the weight of the IBC to a point, after which the thermal limits of the magnetic components restrict any further reduction in size. Additionally, it was shown that for specifications on the lower-end of the voltage/power range, single-phase boost converters are preferable to the interleaved topologies, offering higher power densities across a range of voltage ratios. Conversely, for higher power, higher voltage designs, the interleaved two-phase topologies are superior, offering feasible designs across a wider range of voltage ratios, with the IPT-based design giving the highest power densities. Comparison of the existing prototype design with an optimised design for a 220-600 V, 40 kW, 75 kHz specification indicates that design optimisation techniques have the potential to offer significant improvements in power density, with the optimised design offering a potential reduction in component weight of around 33%.

Broadly speaking, the results indicate that for the range of design specifications and components that were considered, power densities of between 5 and 20 kW/kg are achievable, with corresponding efficiencies in the range of 98-99%. The specific power densities that are achievable heavily depend on the design specification, and it is essential for this to be considered when assessing the design quality of a power converter. If the existing limits of power density are to be further extended, improved device and component technologies are required. In particular, improved magnetic components, with higher temperature cores, improved cooling, and lower losses, may be a key facilitator for increased power density.

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REFERENCES


