Emerging Trends in Silicon Carbide Power Electronics

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Outline

- Motivation for WBG IC design and CAD
- Design flow considerations for WBG IC design
- UA WBG circuits
- Design automation for heterogeneous integration
  - LTCC layout
  - Power module layout synthesis
We Lose a LOT of Energy!

Estimated U.S. Energy Consumption in 2015: 97.5 Quads

<table>
<thead>
<tr>
<th>Category</th>
<th>Processed</th>
<th>Lost</th>
<th>Waste</th>
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</thead>
<tbody>
<tr>
<td>Electric</td>
<td>38 Quads</td>
<td>25.4 Quads</td>
<td>67%</td>
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<tr>
<td>TOTAL ENERGY</td>
<td>97.5 Quadrillion BTUs</td>
<td>59.1 Quads</td>
<td>60%</td>
</tr>
</tbody>
</table>

Total Energy Consumption: 97.5 Quads

Solar 0.532
Nuclear 8.34
Hydro 2.36
Wind 1.82
Geothermal 0.224
Natural Gas 28.3
Coal 15.7
Biomass 4.72
Petroleum 35.4

Energy Services 38.4
Residential 11.3
Commercial 8.71
Industrial 24.5
Transportation 27.7
Rejected Energy 59.1

We Lose a LOT of Energy!
Among the systems needs are:

- Propulsion, climate control, lighting, communications, power distribution, galley, etc.
Charging Electronics

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Alan Mantooth, University of Arkansas
35X Power Density Increase
Electric Power Grid

ELECTRIC GENERATION

COMMERCIAL

RESIDENTIAL

INDUSTRIAL

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2 kW Solar Inverters

GaN-based 2 kW solar inverter at 216 W/in³ (13.2 kW/L)
(photo courtesy of Pilawa – UIUC)

SiC/GaN-based 2 kW solar inverter at 133 W/in³ (8.13 kW/L)
Integration involves combining all of the following in a simultaneous electrical, thermal, and mechanical design:

- Devices
- Device models & modeling of the module
- Thermal management methods, new materials and devices
- Electrical performance (efficiency, integrity, isolation), new materials
- Mechanical performance, new materials
- Layout optimization (current sharing, EMI)
- IC design (supply, driver, control, protection, communication)
- Integration of passives
1. To achieve the best performance out of WBG device advances, attention must be paid to electronic packaging.

2. Reduction of parasitics, higher frequency operation, thermal management, and long-term reliability mandate integration of a variety of technologies beyond the WBG die.

3. This requires advances in materials, packaging processes, and design tools.
Investigation into an array of materials, techniques and processes for high voltage and high temperature packaging:

- 10 kV breakdown passivation material
- SiC die/substrate attach methods (TLP, sintering, solders)
- Wire bondless interconnect
- 3D packaging
IMC Module Design and Layout

- **1200V, 50A SiC Power MOSFETs (Cree)**
- **1200V, 20A SiC Diodes (Cree)**
- **Total: 18 MOSFETs and 18 Diodes**
- **Module Dimension: 124.27mm × 81.8mm × 17.6mm**
- **The module was laid out following switching cell theory to minimize the parasitic inductance**
Solid State Transformers
Three-Level Power Module

- 1200V, 50A SiC Power MOSFETs (Cree)
- 1200V, 20A SiC Diodes (Cree)
- Total: 8 MOSFETs and 12 Diodes
- Module Dimension: 108mm × 88mm
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EV Power Module: 600V, 450A
Destroyed Power Module

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Aftermath

- All four power SiC MOSFETs were destroyed
  - Each MOSFET made a crater in the encapsulent, displacing the Source bond wires.
  - Each device had a $5\Omega - 30\Omega$ short between Gate and Drain.

- All four Cissoid gate drivers were destroyed
  - Significant static current consumption as well as no response to inputs

- All four isolated power supplies were damaged. The damage stopped at the isolation barrier
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Investigation

➢ High $dv/dt$ observed
  • Previous recorded waveforms show $dv/dt$ at 6 V/ns when $V_{DD} = 150$ V. Higher VDD would only increase the $dv/dt$

➢ Glitch condition – loss of control
  • Switching noise fed back into all control signals

➢ Ringing at switching events
The power supply capacitor provided the energy for the module destruction, bypassing the current limit set on the power supply.

Since the circuit gave no warning, and didn’t glitch, the most likely failure was at the gate driver. Either the gate was left floating or was driven high.

Most likely cause is gate driver failure, either from overload or transients on signal pins.
Mitigation

- Protections – IC design contribution
- Better layout to
  - Improve signal integrity
  - Reduce EMI
- Better gate driver IC
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Paragon II Environment

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Navigators

Symbol Editor

Equation Editor

Topology Editor

Simulator Integration
Paragon II Architecture

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Languages

- VHDL-AMS
- Verilog-A/MS

Simulators

- Verilog-A
- Verilog-A/MS
- VHDL-AMS

Paragon II

Model Management
Simulation Management

Parse Translate IN
Lang Code Gen OUT

Editors
Navigators
Utilities
Analysis

Libraries

- Simulink
- Electrical
- Assertions
- Spice
- ED Analog
- User

CMX (standard) Modlyng Data Format XML

Model / Testbench

- Symbol
- Architecture
- Topology
- Configuration
- Equations
- TestB Setup
Models Drive Design Activity

**Models**
- SiC MOS (power and low-voltage)
- SiC diodes
- SiC BJT, SJT
- SiC SIT
- SiC thyristor, GTO
- SiC IGBT (Si/SiC n and p type; over T)
- Si LDMOS
- SiGe HBT
- GaN HEMT
- Patented wide temperature modeling methods (8,608,376)

**Modeling Tools**
- Most advanced device modeling tools (Paragon II)
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SiC Low Voltage MOSFET Model

- Accurate DC and CV characterization method at high temperature
- Verilog-A version development of BSIM470 model using Paragon; Modification for SiC MOSFETs
- Fixed several bugs i.e. C-V at $V_{bs} = 0$ and $V_{ds} = 0$
- A custom IC-CAP module development for parameter extraction and optimization
- Extraction of slow trap information from $I_d-V_g$ characteristics
- Inclusion of new temperature dependent intrinsic carrier concentration model
- Development of body bias dependent mobility model
- New parameter extraction method for body effect modeling
- Modeling of soft transition from triode to saturation
- Modeling of aging
- New strategy for temperature scaling
SiC Low-Voltage Device Model

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Body Effect Modeling

Fitting results – BSIM4:
Body Effect Modeling
Fitting results – this work (PFET):
Body Effect Modeling

Fitting results – this work (NFET):
### Digital:
- **Flyback Controller**
- **ADC Controller**
- **Standard component parts**
  - RS-485
  - Registers
  - Clock Generators

### Analog:
- **Improved PLL (4 MHz)**
- **ADC, DAC**
- **Analog Flyback Controller**

### Gate Driver:
- **Programmable CMOS driver**
- **Linear Regulators**

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#### Table:

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<th>Device Characteristics</th>
<th>Control Functions</th>
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<td>Flyback Controller</td>
<td>Reference Controllers</td>
</tr>
<tr>
<td>Analog Control 1</td>
<td>Flyback Controller</td>
</tr>
<tr>
<td>Flyback Controller</td>
<td>8 Bit SAR ADC</td>
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<tr>
<td>Digital Interface</td>
<td>1 to V Converter</td>
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<tr>
<td>DIP Interface</td>
<td>Switching Control Block</td>
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<tr>
<td>Flyback Controller</td>
<td>Ring Oscillator</td>
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<tr>
<td>Analog Control 2</td>
<td>Clock Generators</td>
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<tr>
<td>PLL</td>
<td>Test Outs 1</td>
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<tr>
<td>Flyback Controller</td>
<td>Test Outs 2</td>
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<tr>
<td>Reference Generators</td>
<td>RS-485 Registers</td>
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<tr>
<td>Power On Chip</td>
<td>2.8 SAR ADC</td>
</tr>
<tr>
<td>Integrated Gate Driver</td>
<td>3.4 Bit Ramp ADC</td>
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<tr>
<td>Digital Controller</td>
<td>ADC Control Logic</td>
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<tr>
<td>Communications Block</td>
<td>RS 485 Receiver</td>
</tr>
<tr>
<td>Communications Block</td>
<td>RS 485 Transmitter</td>
</tr>
</tbody>
</table>
Gate Driver Circuit

- **Variable drive strength**
- **Built-in test**
- **Operational to over 400 °C**

Gate Driver Full Strength Rise and Fall Times

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Rise (ns)</th>
<th>Fall (ns)</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>60</td>
<td>30</td>
</tr>
<tr>
<td>50</td>
<td>55</td>
<td>25</td>
</tr>
<tr>
<td>100</td>
<td>50</td>
<td>20</td>
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<tr>
<td>150</td>
<td>45</td>
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<td>200</td>
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<td>250</td>
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<td>350</td>
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<tr>
<td>400</td>
<td>20</td>
<td>0</td>
</tr>
<tr>
<td>450</td>
<td>15</td>
<td>0</td>
</tr>
</tbody>
</table>
D/A Converter

Features
- 8-bit resolution
- High temperature operation > 400 °C
- ±2 LSB DNL at 400 °C

D/A DNL at 400 °C w/ 5V reference
RS-485 Communications

**Features**
- **Operation up to 400 °C**
- **True Fail-Safe Receiver**
- **Operational over long distances (1200 ft cat5e cable)**

![RS-485 Diagram](image1)

**RS-485 Driver**

![RS-485 Diagram](image2)

**RS-485 Receiver**

![Graph](image3)

**Propagation Delays over Temperature**

- Driver Enable to Output High
- Driver Enable to Output Low
Features

- **Input Voltage Range:** 20 V to 30 V
- **Output Voltage:** 15 V
- **Output Current:** 100 mA
- **Output Voltage Tolerance:** ±2%
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Multi-Chip Power Module Layout Synthesis Tool - PowerSynth

A software tool for the design and layout of multi-chip integrated power modules
Overview of PowerSynth

- Explore the design spaces of integrated power modules
- Uses fast thermal and electrical models to gauge power module performance quickly
- Multi-objective optimization allows for many trade-off design solutions to be considered
- Easily export design solutions to Q3D and SolidWorks
- Current work: Accounting for EMI in layout
Design Flow

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Circuit Schematic

Layout template

Select substrate and components

Assign performance measures (objectives)

Perform Layout Optimization

Explore solution set

Export solutions
- View and sort through performance trade-off data
- Select solution which best suits design problem
- Save multiple solutions back into the Project Builder for more detailed comparison
- Supports 2D and 3D data visualization
- An envelope or window is used to sort through high dimensional data
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Export Designs

- Export to SolidWorks or Q3D
- Further electrical and thermal verification through Q3D and SolidWorks
- Export for manufacturing from SolidWorks
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- Thermal model is within 10% accuracy of FEM model and ~10,000 times faster
- Electrical parasitic model is within 10-20% accuracy for inductance, resistance and capacitance and ~1 million times faster than FEM
- These two fast models allow for multi-objective trade-off curve creation
- Allows for improved visibility of total design space

Characterized temperature distribution for a single device
So, where does modeling, IC design, heterogeneous integration, and multi-objective layout synthesis take us?
An 3D Wire Bondless Half Bridge with Integrated Gate Driver

Top side of interposer with Gate Driver and Passives

Bottom side of interposer with Wire bondless MOSFETs

Functioning module on double-pulse test stand at NCREPT

Alan Mantooth, University of Arkansas
Summary

- Need for higher efficiency is being driven by all sorts of energy demands.
- Heterogeneous integration is being driven by the “need for speed”, which translates into volumetric reduction and higher efficiency.
- Heterogeneous power electronics integration is key to unleashing WBG performance.
- Wide bandgap IC design provides solutions silicon cannot touch.