Reliability and Qualification of Modern Power Devices

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University of Warwick
# Project Team

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<tr>
<th>Warwick</th>
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**Power Semiconductor Devices**

<table>
<thead>
<tr>
<th>Bristol</th>
<th>Newcastle</th>
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<tbody>
<tr>
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**Reliability of Power Modules**

**High Frequency Power Electronics**

**Condition and Health Monitoring**
Work Packages

- **Discrete Device WP1**
  - Warwick, Bristol

- **Module level WP2**
  - Nottingham

- **Gate Driving WP3**
  - Newcastle, Bristol

- **Converter application demonstrator WP4**
  - All
Contents

• Reliability and Qualification
• Electrothermal Robustness
• Temperature Sensitive Electrical Parameters in SiC
# Failure Categorization

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<th>Single Event Failure</th>
<th>Slow degradation/wear-out</th>
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<tbody>
<tr>
<td><strong>Device Failure</strong></td>
<td>• Electrothermal overstress</td>
<td>• Gate oxide degradation from BTI or hot-carrier injection</td>
</tr>
<tr>
<td></td>
<td>• Avalanche breakdown</td>
<td>• Metallization degradation</td>
</tr>
<tr>
<td></td>
<td>• Static/dynamic latching for IGBTs</td>
<td>• Bipolar degradation in SiC</td>
</tr>
<tr>
<td></td>
<td>• Cosmic ray incidents</td>
<td>• Current collapse in GaN</td>
</tr>
<tr>
<td><strong>Packaging Failure</strong></td>
<td>• Thermal Shock</td>
<td>• Solder pad delamination</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Wire bond lift-off</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Baseplate cracking</td>
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</tbody>
</table>
Single-Event Failures

Thermal runaway due to hot-spots and current crowding

\[
\frac{\partial P_{\text{generated}}}{\partial T} > \frac{\partial P_{\text{dissipated}}}{\partial T}
\]

\[
P_{\text{generated}} = V_{DS} \cdot I_{DS}
\]

\[
P_{\text{dissipated}} = \frac{T_j - T_{\text{amb}}}{Z_{\text{thJC}}}
\]

\[
V_{DS} \cdot \frac{\partial I_{DS}}{\partial T} > \frac{1}{Z_{\text{thJC}}(t_{\text{pulse}})}
\]
Power Packaging Failure

- Packaging failure is usually gradual although the end result is catastrophic.

Solder voiding

Wire-bond lift-off resulting from power cycling
Qualification

• JEDEC means the Joint Electron Device Engineering Council and AEC means the Automotive Electronics Council

• Both regulate the standards for **device tests** and **reliability**

• All commercially available devices must pass these tests

<table>
<thead>
<tr>
<th>Test</th>
<th>Component</th>
<th>Stress Point</th>
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<tr>
<td>HTGB (High Temperature Gate Bias)</td>
<td>Device</td>
<td>Gate Oxide</td>
</tr>
<tr>
<td>HTRB (High Temperature Reverse Bias)</td>
<td>Device</td>
<td>Leakage currents</td>
</tr>
<tr>
<td>THBS (Temperature Humidity Bias Stress Test)</td>
<td>Device/Package</td>
<td>Leakage currents</td>
</tr>
<tr>
<td>HS (Hot Storage)</td>
<td>Device/Package</td>
<td>Leakage currents</td>
</tr>
<tr>
<td>TMCL Temperature Cycling</td>
<td>Package</td>
<td>Solder/wirebonds</td>
</tr>
<tr>
<td>Thermal Fatigue (power cycling)</td>
<td>Package</td>
<td>Solder/wirebonds</td>
</tr>
<tr>
<td>Unbiased Humidity Stress Test</td>
<td>Package</td>
<td>Epoxy, Gel etc</td>
</tr>
</tbody>
</table>
Power Cycling in SiC

Power cycling results reported from other researchers show SiC is less reliable using traditional packaging techniques [1]
• This has been reported in [1] and [2]
• SiC has a Young’s Modulus 3 times higher than silicon
• Also, the SiC die is thicker although the electrical drift region is thinner.


Power Cycling in SiC

- SiC MOSFETs are smaller and therefore have greater stresses

- However, recent improvements in solder/die attach technology has improved SiC performance under power cycling

High Temperature Gate Bias

- MOSFETs and IGBTs have MOS gates
- The MOS gate stands for Metal-Oxide-Semiconductor
- The Oxide should be a perfect Insulator
- However, defects in the oxide can cause conduction through the oxide
- All MOSFETs must pass **1000 hours** of the rated gate voltage at 150 °C
- Electrical Parameters (Threshold Voltage) must not shift by more than 25% otherwise it is classified as a fail
High Temperature Gate Bias

\( E_G \): Energy Bandgap  
\( q\chi \): Electron Affinity of the Semiconductor  
\( E_C \): Conduction Band  
\( E_V \): Valence Band  
\( E_F \): Fermi Level

Energy band diagram for p-type MOS capacitor

- \( V_G < 0 \): Accumulation
- \( V_G = 0 \): Flat band
- \( V_T > V_G > 0 \): Depletion
- \( V_G > V_T \): Inversion
High Temperature Gate Bias

- Under high temperature gate bias, traps can form in the oxide
- The traps form through a diffusion process, hence, is temperature sensitive
- These oxide traps increase the fixed oxide trap in the gate insulator
- This can change the threshold voltage of the MOSFET depending on the polarity of the trapped charge

\[
V_{TH} = \left( \Phi_{MS} \pm \frac{Q_F}{C_{OX}} \right) + 2\Phi_B + \frac{\sqrt{2qe_{si}N_A 2\Phi_B}}{C_{OX}}
\]

A reduced threshold voltage is a circuit hazard because of short circuits especially at elevated temperatures
High Temperature Gate Bias

- Because of the wide bandgap (3.4 eV), SiC has a smaller barrier height with SiO$_2$ and is therefore more susceptible to FN tunnelling.

- Si has a smaller bandgap and therefore has larger barrier heights with SiO$_2$.

- For most power electronics engineers, SiC still has to prove itself on HTGB.

![Band offsets of different semiconductors](image1)

![SiC/SiO$_2$ band diagram](image2)
Why do we need Negative $V_{GS}$?

- When high side device is switched, the resulting $dV_{DS}/dt$ coupled with $C_{GD}$ results in a Miller current ($C_{GD}dV_{DS}/dt$).
- This Miller current charges the low side gate capacitance $C_{GS}$.
- If the resulting unintentional $V_{GS}$ exceeds $V_{TH}$, then we have short circuit currents.

$$V_{GS} = R_G C_{GD} \frac{dV_{DS}}{dt} \left( 1 - e^{-\frac{t}{R_G(C_{GD} + C_{GS})}} \right)$$

Why do we need Negative $V_{GS}$?

• Parasitic gate voltages result in short circuit currents

• To prevent this short circuit current, a negative gate voltage can be used for turn-OFF

Parasitic Gate Voltage in SiC

\[ V_{GS} = R_G C_{GD} \frac{dV_{DS}}{dt} \left( 1 - e^{-\frac{-t}{R_G(C_{GD} + C_{GS})}} \right) \]

\[ \frac{C_{GD}}{C_{GD} + C_{GS}} \] is the critical parameter that determines crosstalk
Negative Bias Temperature Instability

- NBTI is the threshold voltage shift due to negative gate bias
- It causes threshold voltage reduction and potential catastrophic failure in high current modules with parallel devices
- It is no longer a major problem in Si IGBTs and MOSFETs
- It is a major problem in SiC power devices (especially for automotive)

Negative Bias Temperature Instability

2. Comparison between Cree’s C3M and C2M SiC MOSFETs

The main difference between Cree’s generation 3 (C3M) and generation 2 (C2M) SiC MOSFET is the gate to source voltage ($V_{GS}$) requirements. As shown in Figure 2 and Figure 3, operational values of $V_{GS}$ for C3M are -4V/+15V while operational values of $V_{GS}$ for C2M are -5V/+20V. This reduction in $V_{GS}$ requirements lowers the overall power losses in Cree’s C3M SiC MOSFET.

<table>
<thead>
<tr>
<th>$V_{GS}$ REQUIREMENTS</th>
<th>C2M MOSFET</th>
<th>C3M MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operational $V_{GS}$</td>
<td>-5V/+20V</td>
<td>-4V/+15V</td>
</tr>
<tr>
<td>Maximum $V_{GS}$</td>
<td>-10V/+25V</td>
<td>-8V/+19V</td>
</tr>
<tr>
<td>Safe Operating $V_{GS}$</td>
<td>0V/+18V</td>
<td>0V/+15V</td>
</tr>
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Figure 2. VGS requirements of Cree’s C2M MOSFET.  Figure 3. VGS requirements of Cree’s C3M MOSFET.

- Wider bandgap in SiC means reduced band offsets and carbon atoms mean higher oxide and interface traps
- Problems have been reported by Infineon, ROHM and CREE
- Reliability tests for AEC Q101 does not include NBTI tests
- Threshold voltage hysteresis means unstable $V_{TH}$ over the life of the application
- In high current modules, the risks of short circuits means on-line detection of $V_{TH}$ shifts is necessary
High Temperature Reverse Bias

- Mobile ions can lodge in the gate oxide and shift the threshold voltage.
- However, defects in the oxide can cause conduction through the oxide.
- All MOSFETs must pass **1000 hours** at 80% of the rated blocking voltage at 150 °C.
- Electrical Parameters (Threshold Voltage) must not shift by more than 25% otherwise it is classified as a fail.
High Temperature Reverse Bias

• HTGB is an important test for detecting ionic contaminants.

• These contaminants will diffuse into the active area under the influence of temperature and high electric fields.

• This occurs in metallisation processes with defects.

• Ionic contaminants can diffuse into the active area and cause localised threshold voltage shifting.
High Temperature Reverse Bias

- Devices that fail under HTRB exhibit significant subthreshold conduction
- Eventually, the devices dissipate significant off-state power dissipation

\[ S_{s-th} = \ln(10) \frac{kT}{q} \left( 1 + \frac{C_d}{C_{ox}} \right) \]
Low Leakage Currents in SiC

- SiC devices have naturally low drain leakage currents compared to silicon devices.

- This is due to low intrinsic carrier concentration hence low rate of carrier generation in the depletion region.

\[
J_L = \frac{n_i}{\tau_{sc}} \sqrt{\frac{2q\varepsilon_{si}}{N_D}} \left( \frac{1}{1 - \alpha_{PNP}} \right)
\]

\[
n_i = \sqrt{N_C N_V} e^{-\frac{E_G}{2kT}}
\]

Low Leakage Currents in SiC

- Due to low leakage currents, SiC are naturally good under series connection.
- Silicon devices show voltage divergence with any slight variation in leakage currents.

Contents

• Reliability and Qualification
• Electrothermal Robustness
• Temperature Sensitive Electrical Parameters in SiC
Unclamped Inductive Switching

The parasitic BJT in the MOSFET can latch with destructive results

- Power MOSFETs have parasitic BJTs
- IGBTs have parasitic thyristors
- Latching of these parasitic components can lead to destructive failure
- SiC devices are more avalanche rugged

The parasitic thyristor in the IGBT can latch with destructive results
Unclamped Inductive Switching

- The avalanche stress test circuit comprises of the power supply, inductor and DUT
- The DUT is used to charge the inductor
- The inductor dissipates energy into the DUT after it is switched off
- The peak avalanche current depends on the inductor charging duration
Unclamped Inductive Switching

- When the parasitic BJT latches, thermal runaway destroys the MOSFET.
- The maximum avalanche energy a MOSFET can sustain depends on the temperature and avalanche duration i.e. size of the inductance

\[ E_{AS} = \frac{1}{2} LI^2 \left( \frac{V_{AV}}{V_{AV} - V_{BUS}} \right) \]

Avalanche Conduction

Unclamped Inductive Switching

Simulated Avalanche current characteristics

Avalanche Conduction through the p-body

BJT Latch-up

Temperature Imbalance under UIS

Switching Imbalance under UIS

Unclamped Inductive Switching

- IGBTs are significantly less rugged than MOSFETs
- This is because there is no internal body diode in IGBTs
- IGBTs have a parasitic thyristor while MOSFETs have a parasitic BJT
- Hence, IGBTs are not considered avalanche capable
- The avalanche ruggedness capability of IGBTs significantly reduce with temperature
3rd Quadrant (Body Diode) Performance

- Only MOSFETs have body diodes
- IGBTs do not hence need discrete diode
- SiC performs best for switching. CoolMOS peak reverse recovery is excessive. Silicon is in the middle.
Body Diode Commutation Failure

- Body-diodes are an integral part of power MOSFETs
- They may be used for intentional reverse current conduction or sometimes can conduct reverse currents un-intentionally
- The body diode is usually a PiN diode and therefore has significant reverse recovery currents

MOSFET schematics showing the body diodes and parasitic BJTs

Body Diode Commutation Failure

• When the body diode conducts in forward mode, there is considerable charge storage in the MOSFET drift region.

• As the diode is turned off, the turn-off $dV/dt$ combined with the drain-to-body capacitance causes a current to flow.

• If the capacitor discharge current and the reverse recovery current is large enough to forward bias the parasitic BJT, then the device can latch with destructive consequences.
Body Diode Commutation Failure

- The test circuit used for assessing the commutation reliability of the MOSFET body diode is shown here:

- It comprises of a high side MOSFET with its body diode used as a free-wheeling diode in a clamped inductive switching setup.

- As the body diode is commutated, the reverse recovery characteristics are assessed.

Body Diode Commutation Failure

- The rate at which the body diode of the MOSFET is switched will determine the peak reverse recovery current.
- The peak reverse current of the CoolMOS device is the highest, followed by the silicon MOSFET and the SiC MOSFET.

SiC MOSFET body diode reverse recovery characteristics for different \( \frac{dI_{DS}}{dt} \)

CoolMOS body diode reverse recovery characteristics for different \( \frac{dI_{DS}}{dt} \)
Body Diode Commutation Failure

• The total reverse recovery charge increases with temperature due to minority carrier lifetime.

• This happens for the silicon MOSFET and CoolMOS device but not the SiC MOSFET.

• SiC MOSFET body diodes have the least switching energy.

![SiC MOSFET body diode reverse characteristics at different temperatures](image1)

![CoolMOS body diode reverse characteristics at different temperatures](image2)
Body Diode Commutation Failure

- The maximum forward current sustainable before latch-up during body diode commutation can be determined experimentally.

- The maximum current decreases with increasing temperature and $dI_{DS}/dt$. 

![SiC MOSFET body diode failure](image1.png)

![CoolMOS body diode failure](image2.png)
Short Circuit Robustness in SiC

• The die size in SiC gives it a higher junction-to-case thermal resistance
• This makes it less robust under short circuit conditions compared to silicon

Contents

- Reliability and Qualification
- Electrothermal Robustness
- Temperature Sensitive Electrical Parameters in SiC
Junction Temperature Sensing

- Custom built sensors designed and integrated with power devices is already an industrial reality. On-chip direct sensor access in IGBT IPM with Fuji Electric, Mitsubishi, Toyota etc.

Mitsubishi 3 kV/300 A SiC Power MOSFET with integrated temperature and current sensors

Toyota IGBT based converters with current and temperature sensors
$R_{DSON}$ vs Temp in SiC MOSFETs

- In high voltage devices where $R_{drift} \gg R_{channel}$, $R_{DSON}$ has a strong PTC.

- In SiC power MOSFETs, where $R_{drift}$ and $R_{channel}$ are comparable, $R_{DSON}$ is non-linear with temperature.

- In new generation SiC trench MOSFETs, where $R_{channel}$ is reduced compared to DMOS devices, $R_{DSON}$ has a more linear relation with temperature (a PTC).

\[
R_{DSON} = \frac{L_{ch}}{W\mu C_{OX}(V_{GS} - V_{TH})} + \frac{L_{drift}}{q\mu N_{DA}}
\]

Decreases with temperature

Increases with temperature

Body Diode Forward Voltage

- The body diode forward voltage is temperature sensitive because of the intrinsic carrier concentration

- It can be used as a TSEP during power cycling

\[ V_{AK} = \frac{2kT}{q} \ln \left( \frac{J_F W_d}{2qD_a n_i F \left( \frac{W_d}{L_a} \right)} \right) \]

Body diode Forward Voltage

- When using the body diode forward voltage as a TSEP during power cycling, it is necessary to use a negative $V_{GS}$ to avoid the body effect.

- The body effect is the coupling between the body diode and the channel. It is peculiar to SiC MOSFETs.

The temperature dependency of the current commutation rate is given by

$$\frac{d^2 I_{DS}}{dt \cdot dT} = V_{GG} e^{-R_G C_{iss}} \left( \frac{d\beta}{dT} (V_{GS} - V_{TH}) - \beta \frac{dV_{TH}}{dT} \right) = \frac{V_{GG} e^{-R_G C_{iss}}}{R_G C_{iss}} \frac{d g_m}{d T}$$

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{d V_{GS}}{dt} \frac{d g_m}{d T}$$

• In SiC devices, unlike silicon, $\frac{d g_m}{d T}$ is positive, hence, $d I / dt$ increases with temperature.
Thermal Effect on Switching Transients

- Impact of temperature on gate current transients
  
  ![Gate Current Transient Graphs](image)

- Impact of temperature on drain voltage transients
  
  ![Drain Voltage Transient Graphs](image)

**SiC Trench**
ON-State Voltage Measurement

- To measure ON-state voltage, high voltage diodes block the main voltage when device is OFF.
- Diodes become forward biased when device is ON.
- Comparator outputs an analogue measurement.
- Current measurements are needed together with ON-state Voltage measurements.
Measuring $dI/dt$ using 4-pin Package

- Using the internal kelvin connection, the voltage drop across the source inductance can act as a TSEP especially in SiC MOSFETs where the switching rate increases with temperature.
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